



Netaji Subhash Engineering college

Techno City, Garia, Kolkata – 700 152

3.3.5 Number of books and chapters in edited volumes / books published, and papers in national/international conference-proceedings per teacher during last five years

A. Books and Chapters in edited volume / books published during the last five years

Sl No.	Name of the Teacher	Title of the book/ chapters published	Title of the paper	ISBN/e-ISBN No.
1	Anupam Ghosh	Advances in Electrical, Electronics, Information, Communication & Bio-Informatics, International Conferences, 2nd 2017 (AEEICB2017),IEEE	Selection of genes mediating human leukemia, using an Artificial Neural Network approach	978-1-5090-5435-0
2	Rajdeep Chakraborty, Runa Seth	Computational Intelligence, Communication, and Business Analytics, Springer	High Entropy and Avalanche Based Non-Feistel Cascaded CFB Block Cipher Through RSBPNDS and TE	978-981-10-6426-5 / 978-981-10-6427-2
3	Chandra Das, Sourav Dutta	Emerging Technologies in Data Mining & Information Security, Springer	SBi-MSREimpute: A Sequential Biclustering Technique based on Mean Squared Residue and Euclidean distance to Predict Missing Values in Microarray Gene Expression Data	978-981-13-1497-1 / 978-981-13-1498-8
4	Anupam Ghosh	Advances In Computing, Communication and Informatics, International Conference, 2016 (ICACCI 2016)(4 VOLS) IEEE	An Improved Fuzzy Based Approach To Impute Missing Values In DNA Microarray Gene Expression Data With Collaborative Filtering	978-1-5090-2030-0
5	Anupam Ghosh	Research In Computational Intelligence and Communication Networks, International Conference, 2 nd 2016, (ICRICN 2016) (CDROM), Springer	An Ensemble Based Missing Value Estimation In DNA Microarray Using Artificial Neural Network	978-981-10-4602-5 / 978-981-10-4603-2

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6	Anupam Ghosh	Advanced Computing & Communication Technology- Proceeding of the 10 th ICACCT, 2016, Springer	Gene Ontology Based Function Prediction of Human Protein Using Protein Sequence and Neighborhood Property of PPI Network	978-981-10-4602-5 / 978-981-10-4603-2
7	Piyali Chatterjee	Proceeding of the 5 th International Conference on Frontiers in Intelligent Computing: Theory & Applications, FICTA 2016, Vol-2, Springer	Gene Ontology Based Function Prediction of Human Protein Using Protein Sequence and Neighborhood Property of PPI Network	978-981-10-3155-6 / 978-981-10-3156-4
8	Piyali Chatterjee	Advanced Computing & Systems for Security, Vol-4, Spinger	Functional Group Prediction of Un-annotated Protein by Exploiting Its Neighborhood Analysis in Saccharomyces Cerevisiae Protein Interaction Network	978-981-10-3390-2 / 978-981-10-3391-9
9	Piyali Chatterjee	Proceeding of the 5 th International Conference on Frontiers in Intelligent Computing: Theory & Applications, FICTA 2016, Vol-2, Springer	PLoc-Euk: An ensemble classifier for prediction of Eukaryotic Protein Subcellular Localization	978-981-10-3155-6 / 978-981-10-3156-4

B. Papers in national / international conference proceedings during the last five years

Sl No.	Name of the Teacher	Title of the paper
1	Chandra Das & Shilpi Bose	NHGSSC: New Hybrid Gene Selection-Sample Classification Method in Microarray Data
2	Chandra Das & Shilpi Bose	An Ensemble Filtering Approach based Supervised Gene Clustering Algorithm to Identify Informative Genes to Improve Sample Classification Accuracy in Microarray Gene Expression Data
3	Atanu Das	A New Method for Tutorial Gap Identification towards Students Modeling
4	Rajdeep Chakraborty, Runa Seth	Design of FPGA Based ECB Cryptosystem: RPPT Embedded with TB
5	Rajdeep Chakraborty, Runa Seth	An FPGA Based Block Cipher through Recursive Positional Substitution on Prime-Nonprime of Cluster (RPSPNC)

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High Entropy and Avalanche Based Non-Feistel Cascaded CFB Block Cipher Through RSBPNDS and TE

Rajdeep Chakraborty¹(✉), Runa Seth¹, and J.K. Mandal²

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Abstract. Security solutions in today's data driven solutions have become an inevitable part. Through this privacy, confidentiality and trust can be achieved and this cascaded technique is proposed. Cryptography is most preferred methods to achieve these goals and cryptography is implemented/realized through applied mathematics. Symmetric key cryptography is most efficient method for the security of big data and almost all established symmetric key algorithms; Triple Data Encryption Standard, International Data Encryption Algorithm, Advanced Encryption Standard; are based on Feistel block cipher. This proposed cascaded technique is a non-Feistel block cipher where plaintext is divided into n number of blocks and each blocks are applied with two encryption functions; Recursive Selected Block Prime-Non-Prime Differential Substitution and Triangular Encryption; in cascaded manner. To achieve good entropy and avalanche; one can apply Cipher Feedback mode to generate final ciphertext by encrypting block by block. This proposed cascaded technique; for its feasibility; is compared with RSA in non-homogeneity, N-gram, floating frequency, avalanche ratio test and entropy test.

Keywords: Symmetric block cipher · Cascading · RSBPNDS · TE · CFB · XOR · Entropy · Avalanche · N-gram · Floating frequency

1 Introduction

The cascaded technique is proposed to achieve the goals of confidentiality, security, privacy and private key based trust/authentication of big data [1–6]. Symmetric key cryptography [6, 8] is efficient accepted methods to achieve this goal. The proposed cascaded technique is non-Feistel block cipher [6] and implemented in bit level to encrypt a big data [5]. Cipher Feedback (CFB) [6] mode is also incorporated to encrypt block by block to get high avalanche ratio and high entropy ratio [3, 6]. Entropy is degree of randomness and it counter many attacks like brute-force-attack, known plaintext attack, known ciphertext attack and plaintext-ciphertext pair attack [6, 10].

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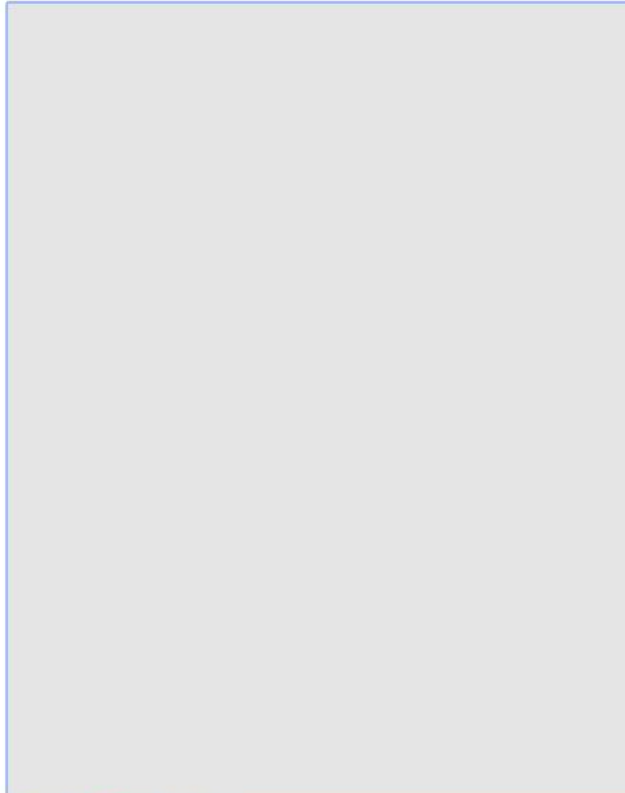
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Sourav Datta, Mihiba Hare, Faraz Ahmad, Anam Saha, Mamraj Kumar and Chandra Das

Abstract Due to technical problems in DNA microarray technology, the output matrix named gene expression data contains a huge number of missing entries. These missing entries create problems when analysis algorithms like classification, clustering, etc. are applied on microarray gene expression data as these methods require complete data matrix. To solve the above-mentioned problem, several missing value imputation techniques have been developed. Among them clustering- and biclustering-based missing value prediction methods are more popular due to their simplicity. In this regard, here a new biclustering-based sequential imputation method is proposed. In this method, for every missing position, a bicluster is formed in a novel manner using the concept of mean squared residue (MSR) score and Euclidean distance. Then the imputation is carried out sequentially by computing the weighted average of the neighbour genes and samples present in the bicluster. To evaluate the

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Preface

This AISC volume contains selected papers presented at the 10th International Conference on Advanced Computing and Communication Technologies (10th ICACCT 2016), technically sponsored by Institution of Electronics and Telecommunication Engineers (India), held during November 18–20, 2016 at Asia Pacific Institute of Information Technology, Panipat, India.

The technical program at 10th ICACCT 2016 featured inaugural addresses by Prof. Lalit M. Patnaik, National Institute of Advanced Studies, IISc, Bangalore and Mr. V. Ramagopal, Executive Director, Panipat Refinery and Petrochemicals, Indian Oil Corporation Ltd., Panipat; followed by six contributed paper sessions; Invited Paper Sessions and a valedictory session. The technical sessions were chaired by Prof. J.K. Mandal, Kalyani University; Prof. Dhananjay Bhattacharyya, Saha Institute of Nuclear Physics, Kolkata; Prof. Anu Mehra, AMITY University, Noida; Dr. Surya P. Singh, Indian Institute of Technology, Delhi; Mr. R. Ramamurthy, Dy. General Manager, Panipat Refinery and Petrochemicals, Indian Oil Corporation Ltd., Panipat; and Prof. Pradosh K. Roy, Asia Pacific Institute of Information Technology, Panipat.

Out of the contributed papers, 150 papers were shortlisted for second and third rounds of review by the expert panel after content evaluation and anti-plagiarism check using Turnitin®. After a rigorous review process, the final selection of 31 papers, corresponding to an acceptance rate of 20% was determined by these evaluation process. The selected papers cover a wide range of topics spanning theory, systems, applications, and case studies that could provide insights for using and enhancing advanced computing systems, communication technologies, services, and facilities.

A review of the state-of-the-art research work together with a discussion on CORDA as a computational model with reference to the problem of multi-robot area coverage has been enlightened in the invited paper.

The development of computational intelligence, it may be recalled, was inspired by observable and imitable aspects of intelligent activity of human being and nature. In the recent years, many hybrid techniques using the theories of computational intelligence are being applied in many fields of engineering and have many other practical implementations. Conforming to the theme of the conference, the

volume includes systems based on computational intelligence on data of various nature, e.g., text mining, image thresholding and encryption, target coverage and localization in wireless sensor networks, dynamic facility layout, human activity recognition, software defect prediction, interactive recommender system, genes mediating leukemia, and glaucoma diagnosis for retinal images. The other chapters relate to knowledge representation and deep learning, innovations in data encryption, reliability in MANET, active filters, innovative antenna design, micro electromechanical (MEM) systems design, quantum dot cellular automata, wave digital filters, heterogeneous distributed computing systems, big data analysis and a seminal paper on statistical machine translation of Bodo language.

We would like to thank members of the advisory and the program committee, especially Prof. Nikhil Ranjan Pal, Indian Statistical Institute, Calcutta; Prof. Subir Sarkar, Jadavpur University, Calcutta; Prof. Partha P. Bhattacharya, Mody University, Sikar, Rajasthan; Prof. Alok K. Rastogi, Institute for Excellence in Higher Education, Bhopal; Prof. Siddhartha Bhattacharya, RCC Institute of Information Technology, Calcutta; Prof. Bijay Baran Pal, University of Kalyani, West Bengal; Prof. R.R.K. Sharma, Indian Institute of Technology, Kanpur; Prof. Sarmistha Neogy, Jadavpur University, Calcutta; Dr. Nitin Auluck, IIT Ropar, Rupnagar; Dr. Surya Prakash Singh, Indian Institute of Technology, Delhi; Dr. Srabani Mukhopadhyaya, BIT Mesra Kolkata Extension Centre, Calcutta; Dr. Mahavir Jhavar, Ashoka University, Sonapat, Haryana; Dr. Tandra Pal, National Institute of Technology, Durgapur; Prof. Atul Sharma, Thapar University, Patiala; Prof. Moirangthem Marjit Singh, Northeast Regional Institute of Science and Technology, Itanagar, Arunachal Pradesh, for their enormous contributions towards the success of this conference. The authors of all contributed papers, the session chairs, and the session coordinators deserve our special thanks. We are thankful to the authors of the selected papers for suitably incorporating the modifications suggested by the reviewers and the session chairs in the scheduled time frame.

Acceptance of the proposal submitted to Springer Science+Business Media Singapore Pte. Ltd. for publication of the proceedings is gratefully acknowledged. We are grateful to the Institution of Electronics and Telecommunication Engineers (India) for technically sponsoring the conference. We are indebted to Mr. Aninda Bose, Senior Editor, Springer India Pvt. Ltd., New Delhi, for his valuable advice on similarity index and the review process. Financial support from Panipat Refinery and Petrochemicals, IOCL, India, in organizing the conference is gratefully acknowledged.

The Organizing Committee patronized by the Managing Committee of APIIT SD India, viz., Mr. Vinod Gupta, Chairman; Mr. Umesh Aggarwal, Vice Chairman; and Mr. Shrawan Mittal, Auditor; supervised by Prof. Virendra K. Srivastava and the Convener, Prof. Sachin Jasuja did a wonderful job in coordinating various activities.

It is our duty to acknowledge the inspiring guidance of Conference General Chair, Prof. Lalit M. Patnaik, Adjunct Professor, National Institute of Advanced Studies, Indian Institute of Science, Bangalore, India, in maintaining the high standards of the conference.

We would also like to thank the student volunteers for their unforgettable, tireless, and diligent efforts.

We hope the proceedings will inspire more research in computation, communication technologies particularly in computational intelligence and metaheuristic algorithms, in the near future.

Panipat, India
Kalyani, India
Kolkata, India
December 2016

Ramesh K. Choudhary
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Message from the General Chair

The 10th International Conference on Advanced Computing and Communication Technologies (10th ICACCT 2016) organized by the Asia Pacific Institute of Information Technology (APIIT) at Panipat during November 18–20, 2016 was primarily aimed at promoting early research on a wide range of topics in computing systems, communication technologies, and facilities. Theories of computational intelligence, it may be recalled, are being applied in many fields of science and engineering and have many other practical implementations. Therefore, the conference also aimed to enable collaborative efforts among researchers with different expertise and backgrounds.

The accepted papers were subjected to pre- and post-presentation plagiarism check and technical review. To ensure that the similarity percentage is consistently maintained within permissible limits, final versions of papers to appear in the proceedings volume were again subjected to similarity index check by Springer independently.

The Editorial Board, Advisory and Program Committee members, reviewers, invited speakers, session chairs, session coordinators, and student volunteers have done their jobs excellently towards the success of the technical program.

As General Chair of Conference, I convey my profuse thanks to Prof. Virendra K. Srivastava for providing all the excellent support from the APIIT SD India Management, which has been very generous in strongly encouraging this Conference. I would like to thank Prof. Nikhil R. Pal, Indian Statistical Institute, Calcutta; Prof. Jyotsna K. Mandal, Kalyani University; Prof. Dhananjay Bhattacharyya, Saha Institute of Nuclear Physics; Prof. Subir Sarkar, Jadavpur University; Prof. Partha P. Bhattacharya, Mody University, Sikar; Prof. Alok K. Rastogi, Institute for Excellence in Higher Education, Bhopal; Dr. Srabani Mukhopadhyay, BIT Mesra, Kolkata Extension Centre; Prof. Sarmistha Neogy, Jadavpur University; Prof. Siddhartha Bhattacharya, RCC Institute of Information Technology, Calcutta; Dr. Nitin Auluck, IIT Ropar, Rupnagar; Dr. Surya P. Singh, IIT Delhi; Prof. Atul Sharma, Thapar University, Patiala; Prof. Marjit M. Singh, NERIST, Itanagar for their valuable time and efforts in organizing the conference

successfully. Finally, my special appreciation goes to Mr. Aninda Bose, Senior Editor, Springer India Pvt. Ltd., New Delhi for his advice.

We are grateful to the Institution of Electronics and Telecommunication Engineers for being the technical sponsors and Panipat Refinery and Petrochemicals, Indian Oil Corporation Ltd., Panipat, for partial financial support.

I am sure this volume will be indispensable for the researchers engaged in computing and communication technologies.

Bangalore, India
December 2016

Lalit M. Patnaik
INSA Senior Scientist and Adjunct Professor
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About the Editors

Ramesh K. Choudhary, former Director, Asia Pacific Institute of Information Technology, Panipat, obtained Ph.D. from VMU, Salem, has co-authored ‘Testing of Fault Tolerance Techniques’ published by Lambert Academic Publishing, Germany. He was the Indian Coordinator, Featured Europe and South Asia MObility Network (FUSION), an ERUSMUS MUNDUS (EU) project to foster partnerships of emerging Asian countries with the EU countries reinforcing the existing collaborations developed through the EU funded projects. He had also significantly contributed to the EU-ASIA mutual recognition of studies in engineering, management, and informatics. He is Fellow of Institution of Engineers (India), IETE, and Members of IEEE, ACM, and Chinese Association for Artificial Intelligence.

Jyotsna Kumar Mandal, former Dean, Faculty of Engineering, Technology and Management, is Senior Professor, Department of Computer Science and Engineering, University of Kalyani, India. He has obtained Ph.D. (Engg.) from Jadavpur University. Professor Mandal has co-authored six books, viz., Algorithmic Design of Compression Schemes and Correction Techniques—A Practical Approach; Symmetric Encryption—Algorithm, Analysis and Applications: Low Cost-based Security; Steganographic Techniques and Application in Document Authentication—An Algorithmic Approach; Optimization-based Filtering of Random Valued Impulses—An Algorithmic Approach; and Artificial Neural Network Guided Secured Communication Techniques: A Practical Approach; all published by Lambert Academic Publishing, Germany. He has authored more than 350 papers on a wide range of topics in international journals and proceedings. His profile is included in the 31st edition of Marque’s World Who’s Who published in 2013. His areas of research include coding theory, data and network security, remote sensing and GIS-based applications, data compression, error correction, visual cryptography and steganography, distributed and shared memory parallel programming. He is Fellow of Institution of Electronics and Telecommunication Engineers, and Members of IEEE, ACM, and Computer Society of India.

Dhananjay Bhattacharyya, Head of Computer Sciences Division, Saha Institute of Nuclear Physics, Calcutta, India, obtained Ph.D. from Indian Institute of Science, Bangalore, and is a postdoctoral fellow from National Institutes of Health, Bethesda, Maryland, USA. Dr. Bhattacharyya's research interest is in understanding structure–function relationship of biological macromolecules, particularly nucleic acids. In this context, he utilizes available crystallographic data to carry out molecular dynamics simulation and ab initio quantum chemical calculations to understand structural stabilization of nucleic acid bases and recognition of nucleic acid by other ligands. In order to understand different structural features of nucleic acids, the CS division at Saha Institute of Nuclear Physics has developed few software tools under his guidance, such as NUPARM, BPFIND, PyrHB Find, etc. Using some of these tools, the CS division has classified structures of different non-canonical base pairs appearing in RNA crystal structures. Dr. Bhattacharyya has successfully guided several doctoral candidates on computational biology and bioinformatics.

Ramesh K. Choudhary
Jyotsna Kumar Mandal
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Advances in Intelligent Systems and Computing

Volume 562

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Advanced Computing and Communication Technologies

Proceedings of the 10th ICACCT, 2016

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Preface

This AISC volume contains selected papers presented at the 10th International Conference on Advanced Computing and Communication Technologies (10th ICACCT 2016), technically sponsored by Institution of Electronics and Telecommunication Engineers (India), held during November 18–20, 2016 at Asia Pacific Institute of Information Technology, Panipat, India.

The technical program at 10th ICACCT 2016 featured inaugural addresses by Prof. Lalit M. Patnaik, National Institute of Advanced Studies, IISc, Bangalore and Mr. V. Ramagopal, Executive Director, Panipat Refinery and Petrochemicals, Indian Oil Corporation Ltd., Panipat; followed by six contributed paper sessions; Invited Paper Sessions and a valedictory session. The technical sessions were chaired by Prof. J.K. Mandal, Kalyani University; Prof. Dhananjay Bhattacharyya, Saha Institute of Nuclear Physics, Kolkata; Prof. Anu Mehra, AMITY University, Noida; Dr. Surya P. Singh, Indian Institute of Technology, Delhi; Mr. R. Ramamurthy, Dy. General Manager, Panipat Refinery and Petrochemicals, Indian Oil Corporation Ltd., Panipat; and Prof. Pradosh K. Roy, Asia Pacific Institute of Information Technology, Panipat.

Out of the contributed papers, 150 papers were shortlisted for second and third rounds of review by the expert panel after content evaluation and anti-plagiarism check using Turnitin®. After a rigorous review process, the final selection of 31 papers, corresponding to an acceptance rate of 20% was determined by these evaluation process. The selected papers cover a wide range of topics spanning theory, systems, applications, and case studies that could provide insights for using and enhancing advanced computing systems, communication technologies, services, and facilities.

A review of the state-of-the-art research work together with a discussion on CORDA as a computational model with reference to the problem of multi-robot area coverage has been enlightened in the invited paper.

The development of computational intelligence, it may be recalled, was inspired by observable and imitable aspects of intelligent activity of human being and nature. In the recent years, many hybrid techniques using the theories of computational intelligence are being applied in many fields of engineering and have many other practical implementations. Conforming to the theme of the conference, the

volume includes systems based on computational intelligence on data of various nature, e.g., text mining, image thresholding and encryption, target coverage and localization in wireless sensor networks, dynamic facility layout, human activity recognition, software defect prediction, interactive recommender system, genes mediating leukemia, and glaucoma diagnosis for retinal images. The other chapters relate to knowledge representation and deep learning, innovations in data encryption, reliability in MANET, active filters, innovative antenna design, micro electromechanical (MEM) systems design, quantum dot cellular automata, wave digital filters, heterogeneous distributed computing systems, big data analysis and a seminal paper on statistical machine translation of Bodo language.

We would like to thank members of the advisory and the program committee, especially Prof. Nikhil Ranjan Pal, Indian Statistical Institute, Calcutta; Prof. Subir Sarkar, Jadavpur University, Calcutta; Prof. Partha P. Bhattacharya, Mody University, Sikar, Rajasthan; Prof. Alok K. Rastogi, Institute for Excellence in Higher Education, Bhopal; Prof. Siddhartha Bhattacharya, RCC Institute of Information Technology, Calcutta; Prof. Bijay Baran Pal, University of Kalyani, West Bengal; Prof. R.R.K. Sharma, Indian Institute of Technology, Kanpur; Prof. Sarmistha Neogy, Jadavpur University, Calcutta; Dr. Nitin Auluck, IIT Ropar, Rupnagar; Dr. Surya Prakash Singh, Indian Institute of Technology, Delhi; Dr. Srabani Mukhopadhyaya, BIT Mesra Kolkata Extension Centre, Calcutta; Dr. Mahavir Jhavar, Ashoka University, Sonapat, Haryana; Dr. Tandra Pal, National Institute of Technology, Durgapur; Prof. Atul Sharma, Thapar University, Patiala; Prof. Moirangthem Marjit Singh, Northeast Regional Institute of Science and Technology, Itanagar, Arunachal Pradesh, for their enormous contributions towards the success of this conference. The authors of all contributed papers, the session chairs, and the session coordinators deserve our special thanks. We are thankful to the authors of the selected papers for suitably incorporating the modifications suggested by the reviewers and the session chairs in the scheduled time frame.

Acceptance of the proposal submitted to Springer Science+Business Media Singapore Pte. Ltd. for publication of the proceedings is gratefully acknowledged. We are grateful to the Institution of Electronics and Telecommunication Engineers (India) for technically sponsoring the conference. We are indebted to Mr. Aninda Bose, Senior Editor, Springer India Pvt. Ltd., New Delhi, for his valuable advice on similarity index and the review process. Financial support from Panipat Refinery and Petrochemicals, IOCL, India, in organizing the conference is gratefully acknowledged.

The Organizing Committee patronized by the Managing Committee of APIIT SD India, viz., Mr. Vinod Gupta, Chairman; Mr. Umesh Aggarwal, Vice Chairman; and Mr. Shrawan Mittal, Auditor; supervised by Prof. Virendra K. Srivastava and the Convener, Prof. Sachin Jasuja did a wonderful job in coordinating various activities.

It is our duty to acknowledge the inspiring guidance of Conference General Chair, Prof. Lalit M. Patnaik, Adjunct Professor, National Institute of Advanced Studies, Indian Institute of Science, Bangalore, India, in maintaining the high standards of the conference.

We would also like to thank the student volunteers for their unforgettable, tireless, and diligent efforts.

We hope the proceedings will inspire more research in computation, communication technologies particularly in computational intelligence and metaheuristic algorithms, in the near future.

Panipat, India
Kalyani, India
Kolkata, India
December 2016

Ramesh K. Choudhary
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Message from the General Chair

The 10th International Conference on Advanced Computing and Communication Technologies (10th ICACCT 2016) organized by the Asia Pacific Institute of Information Technology (APIIT) at Panipat during November 18–20, 2016 was primarily aimed at promoting early research on a wide range of topics in computing systems, communication technologies, and facilities. Theories of computational intelligence, it may be recalled, are being applied in many fields of science and engineering and have many other practical implementations. Therefore, the conference also aimed to enable collaborative efforts among researchers with different expertise and backgrounds.

The accepted papers were subjected to pre- and post-presentation plagiarism check and technical review. To ensure that the similarity percentage is consistently maintained within permissible limits, final versions of papers to appear in the proceedings volume were again subjected to similarity index check by Springer independently.

The Editorial Board, Advisory and Program Committee members, reviewers, invited speakers, session chairs, session coordinators, and student volunteers have done their jobs excellently towards the success of the technical program.

As General Chair of Conference, I convey my profuse thanks to Prof. Virendra K. Srivastava for providing all the excellent support from the APIIT SD India Management, which has been very generous in strongly encouraging this Conference. I would like to thank Prof. Nikhil R. Pal, Indian Statistical Institute, Calcutta; Prof. Jyotsna K. Mandal, Kalyani University; Prof. Dhananjay Bhattacharyya, Saha Institute of Nuclear Physics; Prof. Subir Sarkar, Jadavpur University; Prof. Partha P. Bhattacharya, Mody University, Sikar; Prof. Alok K. Rastogi, Institute for Excellence in Higher Education, Bhopal; Dr. Srabani Mukhopadhyay, BIT Mesra, Kolkata Extension Centre; Prof. Sarmistha Neogy, Jadavpur University; Prof. Siddhartha Bhattacharya, RCC Institute of Information Technology, Calcutta; Dr. Nitin Auluck, IIT Ropar, Rupnagar; Dr. Surya P. Singh, IIT Delhi; Prof. Atul Sharma, Thapar University, Patiala; Prof. Marjit M. Singh, NERIST, Itanagar for their valuable time and efforts in organizing the conference

successfully. Finally, my special appreciation goes to Mr. Aninda Bose, Senior Editor, Springer India Pvt. Ltd., New Delhi for his advice.

We are grateful to the Institution of Electronics and Telecommunication Engineers for being the technical sponsors and Panipat Refinery and Petrochemicals, Indian Oil Corporation Ltd., Panipat, for partial financial support.

I am sure this volume will be indispensable for the researchers engaged in computing and communication technologies.

Bangalore, India
December 2016

Lalit M. Patnaik
INSA Senior Scientist and Adjunct Professor
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Jyotsna Kumar Mandal, former Dean, Faculty of Engineering, Technology and Management, is Senior Professor, Department of Computer Science and Engineering, University of Kalyani, India. He has obtained Ph.D. (Engg.) from Jadavpur University. Professor Mandal has co-authored six books, viz., Algorithmic Design of Compression Schemes and Correction Techniques—A Practical Approach; Symmetric Encryption—Algorithm, Analysis and Applications: Low Cost-based Security; Steganographic Techniques and Application in Document Authentication—An Algorithmic Approach; Optimization-based Filtering of Random Valued Impulses—An Algorithmic Approach; and Artificial Neural Network Guided Secured Communication Techniques: A Practical Approach; all published by Lambert Academic Publishing, Germany. He has authored more than 350 papers on a wide range of topics in international journals and proceedings. His profile is included in the 31st edition of Marque’s World Who’s Who published in 2013. His areas of research include coding theory, data and network security, remote sensing and GIS-based applications, data compression, error correction, visual cryptography and steganography, distributed and shared memory parallel programming. He is Fellow of Institution of Electronics and Telecommunication Engineers, and Members of IEEE, ACM, and Computer Society of India.

Dhananjay Bhattacharyya, Head of Computer Sciences Division, Saha Institute of Nuclear Physics, Calcutta, India, obtained Ph.D. from Indian Institute of Science, Bangalore, and is a postdoctoral fellow from National Institutes of Health, Bethesda, Maryland, USA. Dr. Bhattacharyya's research interest is in understanding structure–function relationship of biological macromolecules, particularly nucleic acids. In this context, he utilizes available crystallographic data to carry out molecular dynamics simulation and ab initio quantum chemical calculations to understand structural stabilization of nucleic acid bases and recognition of nucleic acid by other ligands. In order to understand different structural features of nucleic acids, the CS division at Saha Institute of Nuclear Physics has developed few software tools under his guidance, such as NUPARM, BPFIND, PyrHB Find, etc. Using some of these tools, the CS division has classified structures of different non-canonical base pairs appearing in RNA crystal structures. Dr. Bhattacharyya has successfully guided several doctoral candidates on computational biology and bioinformatics.

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and Applications

FICTA 2016, Volume 2

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Volume 516

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FICTA 2016, Volume 2

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Preface

The volume is a collection of high-quality peer-reviewed research papers presented at the 5th International Conference on Frontiers in Intelligent Computing: Theory and Applications (FICTA 2016) held at School of Computer Engineering, KIIT University, Bhubaneswar, Odisha, India, during 16–17 September 2016.

The idea of this conference series was conceived by few eminent professors and researchers from premier institutions of India. The first three editions of this conference: FICTA 2012, 2013 and 2014 were organized by Bhubaneswar Engineering College (BEC), Bhubaneswar, Odisha, India. Owing to its popularity and wider visibility in the entire country as well as abroad; the fourth edition of FICTA 2015 has been organized by the prestigious NIT, Durgapur, West Bengal, India. All papers of past FICTA editions are published by Springer AISC Series. Presently, FICTA 2016 is the fifth edition of this conference series which brings researchers, scientists, engineers, and practitioners on to a single platform to exchange and share their theories, methodologies, new ideas, experiences and applications in all areas of intelligent computing theories and applications to various engineering disciplines such as computer science, electronics, electrical, mechanical, and biomedical engineering, etc.

FICTA 2016 had received a good number of submissions from the different areas relating to intelligent computing and its applications, and after a rigorous peer-review process with the help of our program committee members and external reviewers (from the country as well as abroad), good quality papers were selected for publications. The review process has been very crucial with minimum 2 reviews each and in many cases 3–5 reviews along with due checks on similarity and overlaps as well. The number of papers received under FICTA 2016 touched 500 mark including the main track and special sessions. The conference featured eight special sessions in various cutting edge technologies of specialized focus which were organized and chaired by eminent professors. The total number of papers received includes submissions from eight overseas countries. Out of this

pool of received papers, only 150 papers were given acceptance yielding an acceptance ratio of 0.4. These papers have been arranged in two separate volumes: Volume 1: 79 chapters and Volume 2: 71 chapters.

The conference featured many distinguished keynote addresses by eminent speakers like Dr. João Manuel and R.S. Tavares, Faculdade de Engenharia da Universidade do Porto, Porto, Portugal on Computational Image Analysis: Methods and Applications; Dr. Swagatam Das, ISI Kolkata on Swarm Intelligence; Dr. Rajib Mall, Information Technology IIT, Kharagpur; Dr. V. Ravi, Centre of Excellence in Analytics Institute for Development and Research in Banking Technology (IDRBT), (Established by RBI, India) Hyderabad; Dr. Gautam Sanyal, Professor, Department of CSE, NIT Durgapur on Image Processing and Intelligent Computing; and a plenary session on ‘How to write for and get published in scientific journals?’ by Mr. Aninda Bose, Senior Publishing Editor, Springer India.

We thank the General Chairs: Prof. Samaresh Mishra and Prof. Jnyana Ranjan Mohanty at KIIT University Bhubaneswar, India, for providing valuable guidance and inspiration to overcome various difficulties in the process of organizing this conference. We extend our heartfelt thanks to the honorary chairs of this conference: Dr. B.K. Panigrahi, IIT Delhi, and Dr. Swagatam Das, ISI Kolkata, for being with us from the very beginning to the end of this conference, and without their support, this conference could never have been successful. Our heartfelt thanks are due to Prof. P.N. Suganthan, NTU Singapore, for his valuable suggestions on enhancing editorial review process.

We would also like to thank School of Computer Engineering, KIIT University, Bhubaneswar, having coming forward to support us to organize the fifth edition of this conference series. We are amazed to note the enthusiasm of all faculty, staff and students of KIIT to organize the conference in a professional manner. Involvements of faculty coordinators and student volunteers are praiseworthy in every respect. We are confident that in future too we would like to organize many more international level conferences in this beautiful campus. We would also like to thank our sponsors for providing all the support and financial assistance.

We take this opportunity to thank authors of all submitted papers for their hard work, adherence to the deadlines and patience with the review process. The quality of a refereed volume depends mainly on the expertise and dedication of the reviewers. We are indebted to the program committee members and external reviewers who not only produced excellent reviews but also did these in short time frames.

We would also like to thank the participants of this conference, who have considered the conference above all hardships. Finally, we would like to thank all the volunteers who spent tireless efforts in meeting the deadlines and arranging every detail to make sure that the conference can run smoothly. Additionally, CSI Students Branch of ANITS and its team members have contributed a lot to this conference and deserve an appreciation for their contribution.

All efforts are worth and would please us all, if the readers of this proceedings and participants of this conference found the papers and conference inspiring and enjoyable. Our sincere thanks goes to all in press, print and electronic media for their excellent coverage of this conference.

We take this opportunity to thank all keynote speakers, track and special session chairs for their excellent support to make FICTA 2016 a grand success.

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Rituparna Chaki
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Advanced Computing and Systems for Security

Volume Four

Advances in Intelligent Systems and Computing

Volume 568

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Advanced Computing and Systems for Security

Volume Four

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Preface

The Third International Doctoral Symposium on Applied Computation and Security Systems (ACSS 2016) took place during August 12–14, 2016 in Kolkata, India organized by University of Calcutta in collaboration with NIT, Patna. The Ca Foscari University of Venice, Italy and Bialystok University of Technology, Poland were the international collaborators for ACSS 2016.

As the symposium turned to its third consecutive year, it has been interesting to note the kind of interests it has created among the aspiring doctoral scholars and the academic fraternity at large. The uniqueness of being a symposium created specifically for Ph.D. scholars and their doctoral research has already established ACSS as an inimitable event in this part of the globe. The expertise of the eminent members of the program committee helped in pointing out the pros and cons of the research works being discussed during the symposium. Even during presentation of each paper, the respective Session Chair(s) had responded to their responsibilities of penning down a feedback for more improvements of the paper. The final version of the papers thus goes through a second level of modification as per the session chair's comments, before being included in this post-conference book.

Team ACSS is always on the look-out for latest research topics, and in a bid to allow such works, we always include them to our previous interest areas. ACSS 2016 had Android Security as the chosen new interest area, thus inviting researchers working in the domains of data analytics, cloud and service management, security systems, high performance computing, algorithms, image processing, pattern recognition.

The sincere effort of the program committee members, coupled with indexing initiatives from Springer, has drawn a large number of high-quality submissions from scholars all over India and abroad. A thorough double-blind review process has been carried out by the PC members and by external reviewers. While reviewing the papers, reviewers mainly looked at the novelty of the contributions, at the technical content, at the organization and at the clarity of presentation. The entire process of paper submission, review and acceptance process was done electronically. Due to the sincere efforts of the Program Committee and the Organizing Committee members, the symposium resulted in a suite of strong

technical paper presentations followed by effective discussions and suggestions for improvement for each researcher.

The Technical Program Committee for the symposium selected only 21 papers for publication out of 64 submissions after peer review. Later 5 more papers were chosen for presenting in the symposium after the authors submitted enhanced versions and those were reviewed again in a 2-tier pre-symposium review process.

We would like to take this opportunity to thank all the members of the Program Committee and the external reviewers for their excellent and time-bound review works. We thank all the sponsors who have come forward towards organization of this symposium. These include Tata Consultancy Services (TCS), Springer Nature, ACM India, M/s Neitec, Poland, and M/s Fujitsu, Inc., India. We appreciate the initiative and support from Mr. Aninda Bose and his colleagues in Springer Nature for their strong support towards publishing this post-symposium book in the series “Advances in Intelligent Systems and Computing”. Last but not least, we thank all the authors without whom the symposium would have not reached this standard.

On behalf of the editorial team of ACSS 2016, we sincerely hope that ACSS 2016 and the works discussed in the symposium will be beneficial to all its readers and motivate them towards even better works.

Kolkata, India
Białystok, Poland
Mestre, Venice, Italy
Kolkata, India

Rituparna Chaki
Khalid Saeed
Agostino Cortesi
Nabendu Chaki

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Agostino Cortesi, Ph.D. is Full Professor of Computer Science at Ca' Foscari University, Venice, Italy. He served as Dean of the Computer Science studies, as Department Chair, and as Vice-Rector for quality assessment and institutional affairs.

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NHGSSC: New Hybrid Gene Selection-Sample Classification Method in Microarray Data

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Abstract: After invention of DNA microarray technology researchers have started to believe it as an effective tool for diagnosis and classification of cancer. The gene expression dataset generated by DNA microarray technology contains expression profiles of huge quantities of genes for samples of very small in numbers. Among these genes, a very small number of genes are informative that means these genes have appropriate discriminating information for cancer sample identification and classification. These genes are considered as key biomarkers. Reliable set of biomarkers finding is an essential task of microarray gene expression data analysis for cancer sample identification and it has great impact on different biomedical fields. In this regard, a new hybrid gene selection-sample classification model (NHGSSC) is proposed here for selection of relevant genes and classification of cancer samples. The proposed hybrid model is a combination of two methods: (1) gene selection (2) sample classification. For gene selection, a new hybrid single filter and α -depth limited best first search based single wrapper method (SF α -BFSSW) is proposed for selection of most relevant subsets. From these subsets highly informative genes are selected by counting frequency of occurrence (FO) of every gene. Then SF α -BFSSW method based ensemble classifier (SF α -BFSSWEC) is built by combining the classifiers created for the selected gene subsets. Prediction accuracy of the proposed model is tested over different microarray data sets by comparing the results with different existing well known algorithms or models. Results demonstrate the superiority of NHGSSC to other existing models.

Keywords: DNA Microarray Technology, Gene expression data, Feature selection, Filter methods, Wrapper methods, Best First Search, Classification

An Ensemble Filtering Approach based Supervised Gene Clustering Algorithm to Identify Informative Genes to Improve Sample Classification Accuracy in Microarray Gene Expression Data

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Abstract: Sample classification is one of the important downstream analysis based application of microarray gene expression data. Using DNA microarray technology it is possible to measure expression level of several thousand of genes for a few numbers of samples. The outcome of microarray technology, gene expression data matrix contains a huge number of genes compared to a limited number of samples and this is a most important problem for sample classification. Most classification algorithms suffer from such a high-dimensional input space. Also a small number of genes contain relevant information for sample classification. In, this regard, a new multi filtering ensemble approach based supervised gene clustering algorithm is proposed here. The proposed method works in two phases. In, the first phase most relevant genes are selected using multi filtering ensemble approach. In the second phase the selected relevant genes are clustered using sample class information to find groups of correlated genes closely associated with the samples categories. Then a number of most significant cluster representatives are selected as features for sample classification. The performance of the proposed algorithm is compared with existing supervised and unsupervised gene clustering algorithms as well as with popular filter based gene selection methods with respect to classification accuracy of k-nearest neighbor, Support vector machine and Naive Bayes classifiers on different microarray gene expression datasets. It has been found that the proposed method significantly outperforms in all cases.

Keywords: DNA Microarray Technology, Gene expression data, Feature selection, Filter methods, Attribute Clustering, Classification

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A new method for tutorial gap identification towards students modeling

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ABSTRACT

Students modeling is an integral part of any form of education and this becomes more challenging with the advent of new tools of ICT especially Intelligent Tutoring Systems (ITS). Educators must have to take help of such tools to identify the curriculum gaps towards Outcome Based Education (OBE). One of the ways to reduce such gaps is to identify the personalized requirements of tutorials for learners after going through some topics divided into subtopics. This paper proposes a technique to identify the personalized tutorial gaps by analyzing the responses provided by students against MCQ type questions. The proposed method has been implemented within a web based environment. Prototype of the tool having integrated with the proposed method shows that the students can identify their tutorial requirement without the help of human tutor and hence discovering the student's understanding.

Keywords: ICT, OBE, Tutorial, Gap, Students Modeling.

1. INTRODUCTION

Educational world has been experiencing a paradigm shift from teacher centric education to outcome based education (OBE) [1-3] during last two decades. OBE has become accreditation requirements through out the world. OBE ensures cyclical processes which gurantes continuous improvement towards excellence. These cyclical processes involve implementing different mechanism for efficient student modeling. Students performances can not be enhanced unless such modeling is not assured at least at some desired level.

A student model is a representation of student understanding of a topic being taught. The model constructed by human tutors become more accurate with the experiences of the tutor. Such model construction is a difficult task and varies with teaching domains and teaching experiences. Often Intelligent Tutoring Systems (ITS) [5] have been used since the advent of using ICT tools for education for standardization of students modeling. Such models are used as personalized cognitive tool within the Intelligent Learning Environment (ILE).

There are several knowledge components within the representation of the students model. According to curriculum requirements, some components are required to be achieved by tutorials. But requirements of tutorials is not defined a priori in the curriculum most of the times and decided by human tutor as per his own experiences not according to learner's personalized model requirements.

This work advocates the use of automated ICT tools, if not ITS, for identifying personalized tutorials requirement gaps

after going through some set of topics (defined in the curriculum) or subtopics (subdivisions of topic). This identification could be achieved by analysing the responses of the students on a simple web based well designed MCQ test. There are two challenges in these endeavour. First is to design the MCQ test questions having one-to-many relationship maping with the subtopic level content. Second step is to analyse the responses corresponding to the questions to identify knowledge gap (also treated as curriculam gap) which could be fullfilled through the tutorial works specially. The last challenge has been focused in this work mostly.

2. RELATED WORKS

With the advent of OBE [1-3], education systems turning to exhibit more professionalism as expected in the developing economies. Outcome becomes the primary focus in these systems and accreditation requirement enforces to measure the same from a good number of parameters [1] among which one crucial is initiatives taken to bridge the curriculum gap besides competency assessments [6-9] of students after curriculum execution. One well known curriculum components are tutorial often ignored by human tutors because of shortage in time mostly. But even if time is strictly allocated for the same, inexperience teachers could not identify or wrongly identify the topics or subtopics on which tutorials classes need to be conducted at least for majority of students if not for all. Even though the teacher is having huge experience, he needs to analyse intelligently

each individual student before moving in to tutorial classes. To reduce the overload of human tutors, ICT based ITS [5] have been evolved which often took part in student modelling using knowledge based machine learning techniques.

It has been observed that construction of student model is a time-consuming task. Normally this is based on expert human inputs [14]. Structured interviews are conducted and the inputs are lucidly analysed for the same. Crucial instructional implications show that human engineering towards these models disregard the peculiarities between content and learning [11-12]. Learning Factor Analysis (LFA) [13] is another technique where automated search techniques are implemented for identification of knowledge components of the students' model. However, LFA conducts search processes in the closed periphery of human supplied factors. Nevertheless, these methods are somehow dependent on machines learning techniques [10] including complex mechanism.

To reduce these complexities, we propose a technique based on the analysis of student's responses on MCQ questions since the scope of this work is to model the student's tutorial requirements. The proposed scheme is somehow adhoc and expressive but includes procedural approaches.

3. PROPOSED METHOD

The curriculum gap identification required for OBE assessment has been considered here using identification of required tutorials as one of the crucial curriculum components. Educational delivery of the proposed system has been planned considering to the following processes.

1. Dividing the syllabus of a course into several topics as per lecture/delivery plan.
2. Delivery of contents on subtopics (unit of content delivery) of a topic.
3. Generation of MCQ questions set comprising questions having one-to-many relationship with the subtopics.
4. Conducting MCQ test for the students and collecting the question wise responses of the students.
5. Processing the student's responses to identify subtopics wise gap to be filled by tutorials based on some predefined threshold.

The scheme of the processing in the stage 5 is depicted below:

We consider a course with m modules. Now each module M_i , ($1 \leq i \leq m$) is divided into n number of topics. This method is going to operate on a particular topic $Topi_{ij}$, ($1 \leq j \leq n$). Each $Topi_{ij}$ is divided into p subtopics. A subtopic is denoted by $Sutopi_{ijk}$, ($1 \leq k \leq p$).

After completion of the delivery of contents on each subtopics of the topic $Topi_{ij}$ to a student, the student has to give test on question set Q_{ij} which is set on the subtopics of $Topi_{ij}$. Q_{ij} comprises of v number of questions. Each question Q_{ijz} , $1 \leq z \leq v$, in Q_{ij} can be set on one or more subtopics of $Topi_{ij}$.

We use a $v \times p$ matrix $MQSutopi$ showing the mapping between v questions in Q_{ij} and p subtopics.

$MQSutopi [r] [s] = 1$, if Q_{ijr} is set on $Sutopi_{ijs}$,

$MQSutopi [r] [s] = 0$, otherwise, for $1 \leq r \leq v$ and $1 \leq s \leq p$.

$MESutopi [r] [s] = 1$, if $MQSutopi[r][s]=1$ and the student has given correct answer to question Q_{ijr} , set on subtopic $Sutopi_{ijs}$.

$MESutopi [r] [s] = 0$, otherwise, for $1 \leq r \leq v$ and $1 \leq s \leq p$.
 $CASutopi[t] =$ Total number of 1's present in the t^{th} column of matrix $MESutopi$.

We maintain an array $CASutopi$ (decision variable) of size p such that for $1 \leq t \leq p$. It may be noted that total number of 1's present in the t^{th} column of matrix $MESutopi$ signifies how many questions on subtopic $Sutopi_{ijt}$ are correctly answered by a student. If the value in $CASutopi[t]$ is less than threshold Th_{ijt} , then we find a tutorial gap in subtopic $Sutopi_{ijt}$ for the student and assign tutorials to the student on subtopic $Sutopi_{ijt}$.

The threshold plays very important role in this method. Threshold normally decided according to two aspects: (1) academic level (e.g. age, class etc.), (2) academic standard (e.g. rank of the institutes in global or national scenarios). If same content and test questions are used for this purpose, the threshold could vary with respect to academic levels. For example, school educators will use low threshold compared to college level institutes or UG level will set low threshold compared to PG courses.

On the other hand, if the same system is used in different institutes, they should have the liberty to set the threshold according the quality of education they are expecting. OBE also advocates continuously improving the quality of the outcome and hence they need to increase the threshold gradually according to educational objectives, mission and vision of the institutes.

4. IMPLEMENTATION

The proposed technique is implemented using a web based system developed using PHP-MySQL technology using WAMP server at the back and functioning like an small ITS. Such technology has been chosen because of their simplistic nature and easiness from developer's perspective. Since the focus is to implement the tutorial gap identification scheme, the content delivery parts of the proposed system is not discussed and presented here. Following figure 1 presents the simple interface of implementation of test students need to undergo inside the system as an evidence of conducting test and collecting responses using an automated system.

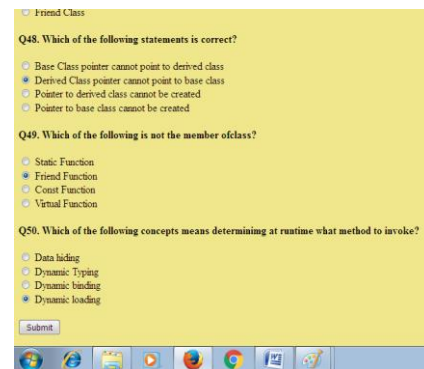


Figure 1. Evidence of conducting MCQ Test

The following figure 2 presents the interface of subtopic wise analysis report according to the proposed scheme.

The following figure 3 presents the interface of the proposed system providing discovered instructions to the students about their tutorial requirements so that they can go through the required tutorials and offering the educational outcome as expected from the system as per regulatory framework.

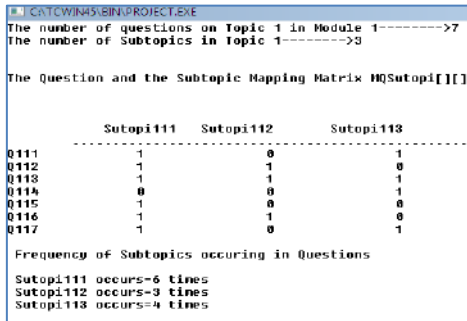


Figure 2. Subtopic wise analysis of responses to MCQ questions

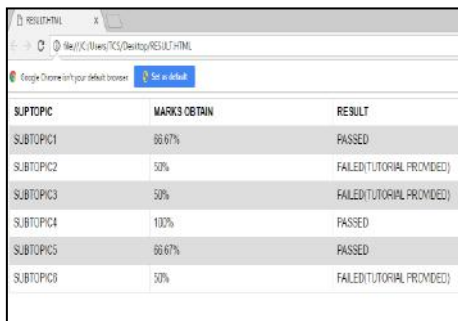


Figure 3. Recommendation report based on analysis using proposed method

The prototype of the proposed system (integrated with the identification scheme), can be improved to work more fruitfully having many features of ITS.

5. RESULTS AND DISCUSSIONS

The developed web based tool was examined through some testing procedure. Though the proposed technique can be used for tutorial gap identification irrespective of any level of education having computer literate target students, the testing was focused on 2nd and 3rd year Computer Science and Engineering students. First experiment conducted with the 50 students of second year Computer Science and Engineering divided into two groups on the course computer organization. It has been observed that the developed method could identify one or more tutorial gap predefined while designing the content and agreed on the MCQ questions for 75% cases. Second experiment conducted on the same set up on third year student on the course operating system but result shows that in around 80% cases predefined gap has been identified. Result of identification observed to be poor a little for 2nd year due to heterogeneous background on account of lateral entry students' consideration perhaps.

So, we can say that the proposed scheme found efficient at least for engineering education. Further experiment on this regard is yet to be conducted for others educational scenarios. It is also expected that the results may further be improved if

better care is taken while design the instructional materials and questions set. On this view, research may further be extended towards standardization of personalized content and questions which was beyond the scope of this venture.

6. CONCLUSIONS

This paper contributes to the literature by proposing a new technique for curriculum gap identification through tutorial recommendation. This paper also advocates the use of automated ICT based tools for such gap identification. This ICT based tools will be able to overcome the limitations of human tutors having diversified experience and teaching styles. Personalized students' models could be presented having deficiencies pointed there in with the help of the use of ICT tools integrated with the proposed technique. Extended version of this proposed technique can be integrated within an ITS so that learning experience could be made better and convert it as ILE. Not only ITS implementation, but conceptualization of the method can improve the teaching performance and hence students' performance with respect to OBE. More use of machine learning and pattern recognition techniques can uplift the work to a level where professional success of educators will not be far away.

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An FPGA Based Block Cipher through Recursive Positional Substitution on Prime-Nonprime of Cluster (RPSPNC)

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ABSTRACT

The technique considers the plaintext as a stream of finite number of bits N , and is divided into a finite number of blocks, each also containing a finite number of bits n , where $1 \leq n \leq N$. Here orientation of the position of bits within a block is performed through a generating function. If the operation is repeated using the same generating function, the original block is regenerated after a finite number of iterations forming a cycle. For a particular length of block, the block itself is regenerated after a finite number of such iterations. Any of the intermediate blocks within this cycle is considered to be the encrypted block. To decrypt the encrypted block from the ciphertext, the same process is to be followed but the process using same generating function is to iterated for different number of times. To achieve the security of a satisfactory level, it is suggested that various blocks or blocks should be of different sizes. The technique does not incur any storage overhead. The technique generates a large key space, so that the chance of breaking the ciphertext is difficult by any technique of cryptanalysis. The implementation on practical scenario is well proven with positive outcome.

Keywords: FPGA, Symmetric Block Cipher, Prime Numbers, VHDL, Synthesis

I. INTRODUCTION

Lack of security may exist when a volume of data is transferred from its source to the destination if no measure is taken for its security. For one reason or the other, most of the data being transmitted must be kept secret from others [3,6]. A very important reason to encode data or messages is to keep them secret. From e-mail to cellular communication, from secured web access to digital cash, cryptography [3,6] is an essential part of today's information systems. It can prevent fraud in electronic commerce and assure the validity of financial transactions. It can prove one's identity and protect one's anonymity. These electronic commerce schemes may fall fraud through forgery, misrepresentation, denial of service and cheating [3,6] if we do not add security to these systems. In fact, computerization makes the risks even greater by allowing attacks that are impossible in non-automated systems. Only strong cryptography can protect against these attacks.

The Section II of this paper deals with the proposed scheme. A concept of key-generation is given in Section III. Section IV describes the implementation through an

FPGA-based system. Results and comparisons are illustrated in Section V. Conclusions are drawn in Section VI.

II. THE TECHNIQUE RPSPNC

The generating function $t=g(s)$, [6] where 's' is the source stream and 't' is the target stream/intermediate block, the generation function orients the positions of different bits, is applied on a block of size n to generate an intermediate block of the same size. The target stream/intermediate block t is generated by the following rules:

1. A bit in the position i ($1 \leq i \leq n-2$) in the block s becomes the bit in the position $(n-i)$ in the block t , if $(n-i)$ is a non-prime integer [1,2].
2. A bit in the position i ($1 \leq i \leq (n-2)$) in the block s becomes the bit in the position j ($1 \leq j \leq (n-i-1)$) in the block t , where j is the precedent prime integer (if any) of $(n-i)$, if $(n-i)$ is a prime integer [1,2].
3. A bit in the position n in the block s remains in the same position in the block t otherwise.
4. A bit in the position $(n-2)$ in the block s is transferred in the block t to the position unoccupied by any bit after rules 1, 2 and 3 are applied.

The technique is illustrated using a flow diagram given in figure 1.

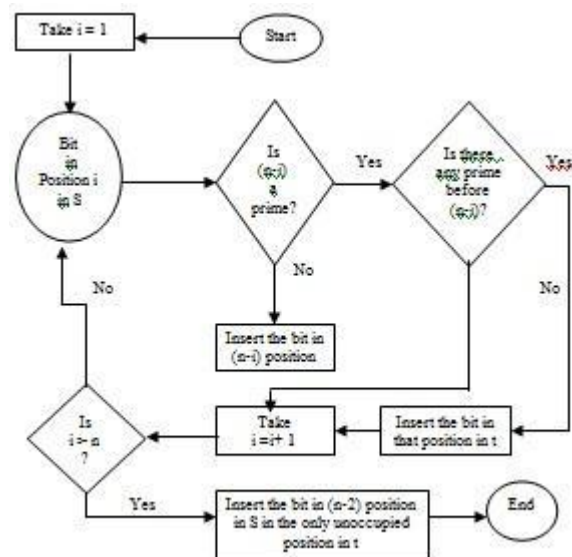


Fig. 1. Overview of RPSPNC

Subsection A. gives the process of encryption, subsection B. gives the decryption process and subsection C. illustrates one example.

A. Encryption

The process of encryption [3,6] is the sub set of the entire set of iterations to form the cycle for a given block. Any intermediate block, t, during the process of forming the cycle may be considered as the encrypted block. Hence if the number of iterations required to form the cycle is ‘i’ for a block of size n, the number of intermediate blocks generated in the cycle is (t), because each iteration generates one block and the final iteration generates the same source block.

B. Decryption

Process of decryption [3,6] is also a sub set of the entire set of work required to form the cycle for the block. The only difference is that one intermediate block of the cycle (the encrypted block) is considered to be the source block in the process of decryption. If the block generated after the tth iteration in the cycle (1 <= t <=(i-1)), ‘i’ being the total number of iterations required to form the cycle, is considered to be the encrypted block, number of iterations required to decrypt the encrypted block is (i-t).

C. Example

Reorientation of bits in a finite length of block can be explained better with an example. Let us consider the block s = 01001011 of size 8 bits.

Source Block							
0	1	0	0	1	0	1	1
1	2	3	4	5	6	7	8
Block After 1 st Iteration							
1	1	0	0	0	1	0	1
1	2	3	4	5	6	7	8
Block After 2 nd Iteration							
0	0	0	0	1	1	1	1
1	2	3	4	5	6	7	8
Block After 3 rd Iteration							
1	1	0	0	0	0	1	1
1	2	3	4	5	6	7	8
Block After 4 th Iteration							
1	0	0	0	1	1	0	1
1	2	3	4	5	6	7	8
Block After 5 th Iteration (Source Block)							
0	1	0	0	1	0	1	1
1	2	3	4	5	6	7	8

Fig. 2. Target block is generated from source block

Table I

Illustration of Mapping (s → t) for Block of Size 8

s	t	Mapping logic from s to t
1	5	Here 8 – 1 = 7, a prime; the precedent prime of 7 is 5
2	6	Here 8 – 2 = 6, a non-prime
3	3	Here 8 – 3 = 5, a prime, the precedent prime of 5 is 3
4	4	Here 8 – 4 = 4, a non-prime
5	2	Here 8 – 5 = 3, a prime, the precedent prime of 3 is 2
6	?	Here 8 – 6 = 2, a prime, there is no precedent prime, allocation suspended
7	1	Here 8 – 7 = 1, a non-prime
8	8	Here 8 being the position of the LSB, no change in position
6	7	One allocation was suspended earlier; since the position 7 is only the unoccupied position so far, that allocation is made there

Figure 1 demonstrates the different intermediate blocks and the target block generated during the cycle.

The Flow diagram to show how positions of the bits of ‘s’ and the different intermediate blocks can be reoriented to complete the cycle is shown in figure 2.

Here since number of iterations (t) [5,6] required to form the cycle is 5, the tth block may be considered as the encrypted block, where ‘t’ ranges from 1 to 4.

How the mapping of source block ‘s’ to a target block ‘t’ is illustrated in table I.

III. THE KEY GENERATION

In the proposed scheme, eight rounds have been considered, each for 2, 4, 8, 16, 32, 64, 128, and 256 block size. Each round is repeated for a finite number of times and the number of iterations will form a part of the encryption-key [2,3,6]. Although the key may be formed in many ways, for the sake of brevity it is proposed to represent the number of iterations in each round by a 16-bit binary string. The binary strings are then concatenated to form a 128-bit key for a particular key. Subsection A. illustrates the key generation process.

Table II

Representation of number of iterations in each round by bits

Round	Block Size	Number of Iterations	
		Decimal	Binary
1.	256	50021	1100001101100101
2.	128	49870	1100001011001110
3.	64	48950	1011111100110110
4.	32	44443	1010110110011011
5.	16	46250	1011010010101010
6.	8	4321	0001000011100001
7.	4	690	0000001010110010
8.	2	72	000000001001000

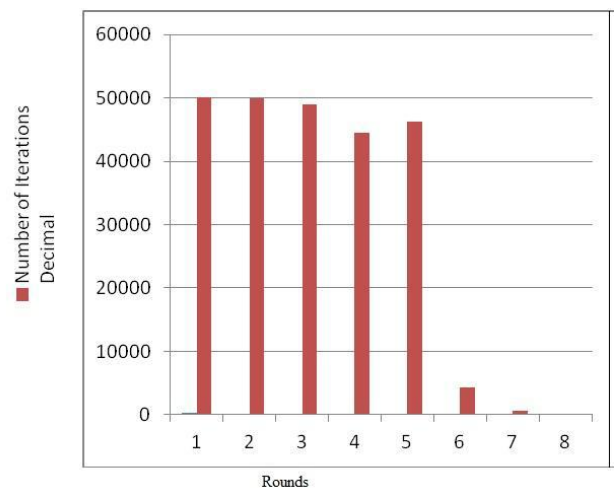


Fig 3. Round v/s iteration

A. EXAMPLE

Consider a particular session [1,3,6] where the source file is encrypted using iterations for block sizes 2, 4, 8, 16, 32, 64, 128, and 256 bits, respectively. Table II shows the corresponding binary value for the number of iterations in each round. Figure 3. shows the graph for the round v/s iteration. When the block size is 2-bit then the process of RSPNC is applied 72 times, for 4-bit block size the process of RSPNC is applied 690 times, similarly when the block size is 256-bit then the process of RSPNC is applied 50021 times. The number of times of iteration is solely decided by the user or sender of the secret message.

These numeric values are converted to equivalent binary strings and these binary strings are concatenated together to form the 128-bit binary string:

```
110000110110010111000010110011101011111001101
1010101101100110111011010010101010000100001110
00010000001010110010000000001001000.
```

This 128-bit binary string will be the key for encryption for a particular session. During decryption, the same key is taken to iterate each round of modulo-subtraction for the specified number of times.

IV. IMPLEMENTATION

This technique has been implemented in C and then feasibility study has been performed. Finally, FPGA [4,6] based implementation has been done in VHDL [5]. In both implementation, the technique takes input from file as a source stream and encryption is performed. The cipher text generated is finally written in another file. The data blocks (8, 16, 32, 64, 128 and 256-bits) from the input file have been stored in array. Then encryption is performed and also stored in array. The reading and writing of data from and in file is based on 8-bit ASCII codes [2,6]. Xilinx ISE 8.1i [4,5,6] software has been used for writing codes in VHDL.

Figure 4 gives the implementation of RSPNC entity and its function. The encryption/decryption entity input bit vector (16-bit), output bit vector (16-bit), key bit vector (8-bit) and EN_DN signal. If EN_DN = 1 then encryption is performed else decryption is performed. During encryption the input bit vector of 16-bits is the plaintext and output 16-bit vector is the ciphertext where as EN_DN value is '1'. During decryption the input bit vector of 16-bits is the ciphertext and the output 16-bit vector is the plaintext where as EN_DN value is '0'. Figure 5 shows the top RTL diagram of RSPNC [4,5,6].

When EN_DN = 1, the 'RSPNC_Encryption' function is called with the parameters, 'varin_bits' which is the plaintext, 'varout_bits' which is the ciphertext, both of these are of 16-bits and third parameter is the 'key_bits' which is the session key of the encryption of 8-bits. When EN_DN = 0, the 'RSPNC_Decryption' function is called with the parameters, 'varin_bits' which is the ciphertext, 'varout_bits' which is the plaintext, both of these are of 16-bits and third parameter is the 'key_bits' which is the session key of the decryption of 8-bits. This code is written in VHDL using behavioral model of coding. The 'RSPNC_VHDL' entity in this

coding has three ports, 'input_bits' of IN type of bit vector of 16-bits, 'output_bits' of OUT type of bit vector of 16-bits, 'key_bits' of IN type of bit vector of 16-bits and 'EN_DN' bit of IN type. 'Behavioral' is the architecture of the entity 'RSPNC_VHDL', this architecture contains a process which is called on the signal 'EN_DN' that is whenever there is a signal in 'EN_DN' this process is called. This process contains two functions, 'RSPNC_Encryption' and 'RSPNC_Decryption'. These two functions are called according to the value of signal bit 'EN_DN' which is already discussed. The implementation here is both functional and files type. These means that the code can be implemented in Xilinx FPGA and the simulation takes the input from a text file and the output is written into another text file. There are various libraries are used, library 'std' and library 'ieee', it is important to note that library 'ieee.std_logic_TEXTIO.all' is used for the implementation of text file reading and writing.

```
library std;
library ieee;
use ieee.std_logic_arith.all;
use work.pack.all;
use std.textio.all;
use ieee.std_logic_TEXTIO.all;
entity RSPNC_VHDL is
Port ( input_bits : in BIT_VECTOR (16 downto 1);
        output_bits : out
        BIT_VECTOR (16 downto 1); key_bits : in
        BIT_VECTOR (8 downto 1);
        EN_DN : in BIT);
end RSPNC_VHDL;
architecture Behavioral of RSPNC_VHDL is
begin
process(EN_DN)
variable varin_bits,varout_bits: bit_vector(16 downto
1);
begin
if (EN_DN='1')then varin_bits:=input_bits;
AA:
RSPNC_Encryption(varin_bits,key_bits,varout_bits);
output_bits<=varout_bits;
else
BB:
RSPNC_Decryption(varin_bits,key_bits,varout_bits);
output_bits<=varout_bits;
end if;
end process;
end Behavioral;
```

Fig 4. RSPNC entity and its function

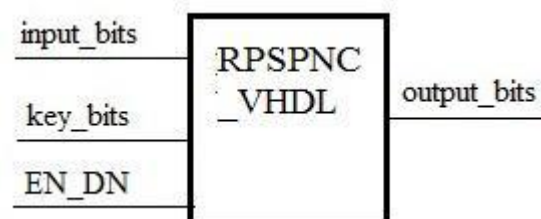


Fig 5. Top level RTL design of RSPNC

V. RESULT AND COMPARISONS

The main emphasis is given on comparisons with RSA. Subsection A gives RTL simulation based results, subsection B gives frequency distribution graph, subsection C gives non-homogeneity test, subsection D deals with time complexity analysis and subsection E chalk out the avalanche ratio test.

A. RTL SIMULATION BASED RESULT

In this section gives some of the results found after implementing RSPNC in VHDL. After synthesizing simulating the code in Xilinx 8.1i [4,5,6]. The main objective is to find an efficient FPGA-based cryptographic technique for implementation in embedded systems.

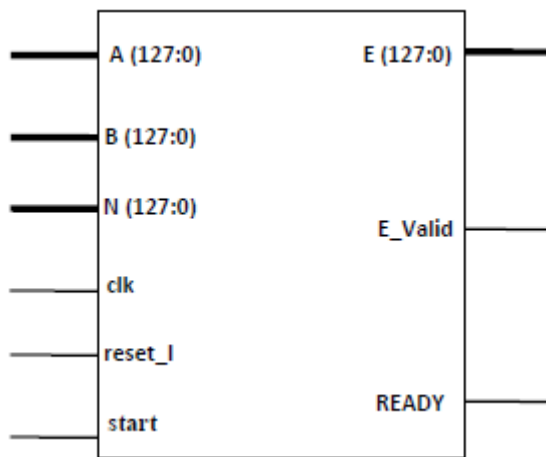


Fig 6. RTL diagram of RSA

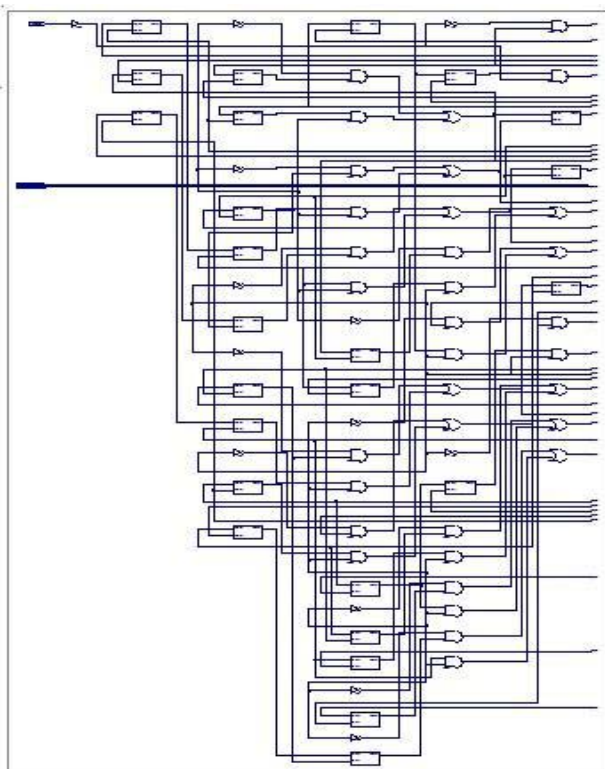


Fig 7. RTL diagram of RSPNC

Table III

HDL synthesis report (Netlist generation of RSA and RSPNC)

Sr No.	Netlist Components	Number	
		RSA	RSPNC
1	ROMs/RAMs	430	110
2	Adders/Subtractions	3	70
3	Registers	420	770
4	Latches	80	80
5	Multiplexers	120	120

Table IV

HDL synthesis report (Timing summary of RSA and RSPNC)

Sr No.	Timing Constraint	Values	
		RSA	RSPNC
1	Speed Grade	-5	-5
2	Minimum period	9.895ns	9.55ns
3	Maximum Frequency	101.06 MHZ	101.06 MHZ
4	Minimum input arrival time before clock	6.697ns	6.55ns
5	Maximum output required time after clock	4.31ns	4.30ns

The design of RSPNC is done using VHDL and implemented in Xilinx Spartan-3E XC3S100E-5VQ100 (package: VQ100, speed grade: -5) FPGA using the ISE 8.1i design tool. Figure 6 shows the RTL of RSA figure 7 shows the RTL of RSPNC.

Table III gives the HDL synthesis report, specifically net list generation [4,5,6] of RSA and RSPNC. RSPNC uses 110 ROMs/RAMs where as RSA uses 430 ROMs/RAMs, RSPNC uses 70 adders/subtractions where RSA uses only 3 adder/subtractions, RSPNC uses 770 registers where as RSA uses 420 registers, both RSPNC and RSA uses 80 latches and 120 multiplexers. Therefore RSPNC is well comparable with RSA.

Table IV gives the HDL synthesis report specifically timing summary [4,5,6] of RSA and RSPNC. The minimum period of RSA is 9.895ns and RSPNC is 9.55ns, minimum input arrival time before clock of RSA is 6.697ns and RSPNC is 6.55 ns and maximum output required time after clock of RSA is 4.31ns and RSPNC is 4.30ns. This implementation has been made on speed grade of -5 and maximum frequency of 101.06 MHZ. Therefore we can say that RSPNC is giving much better result than that of RSA and RSPNC is well comparable with RSA.

B. FREQUENCY DISTRIBUTION GRAPH

The frequency distribution [2,6] is the distribution of the all 256 ASCII characters in the respective files. The degree of cryptanalysis is measures by this method and it is another cryptographic parameter.

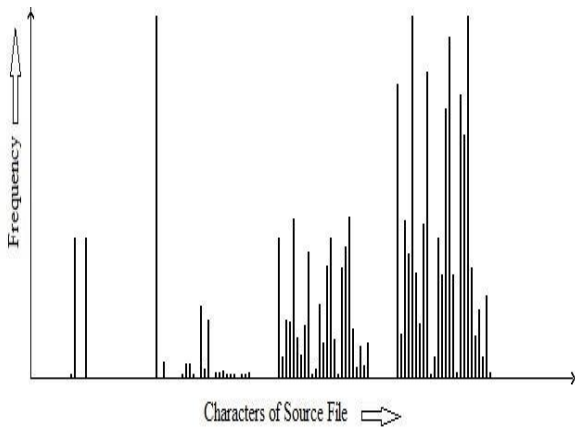


Fig 8. Frequency distribution of source file

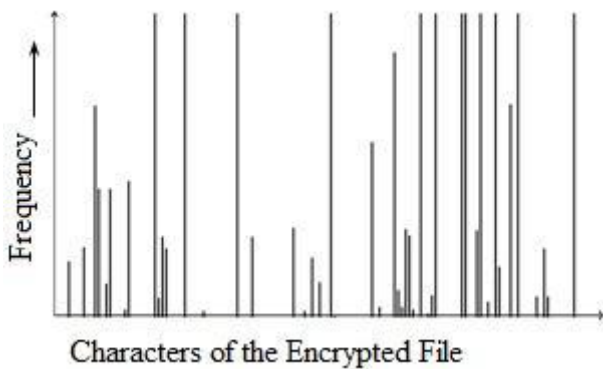


Fig 9. The frequency distribution graph of RSA encrypted file

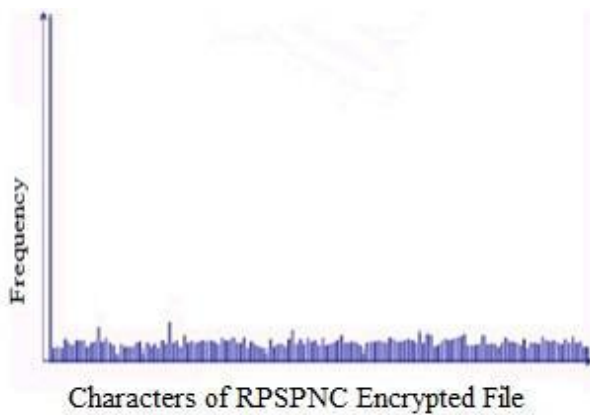


Fig 10. The frequency distribution graph of RPSNPC encrypted file

Figure 8 gives the frequency distribution graph of source file, figure 9 shows the same for RSA encrypted file and figure 10 shows the same for RPSNPC encrypted file. Thus frequency distribution graph of RPSNPC is well comparable with RSA.

C. NON-HOMOGENEITY TEST

Chi-square test [2,6] is performed to find the non-homogeneity [2,6] of RPSNPC with RSA. Ten files of different file typed and different file sizes are taken for this test.

Table V
Chi-Square values of RSA and RPSNPC

Source File	File Size (Bytes)	Chi-Square Values		Degree of freedom	
		RSA	RPSNPC	RSA	RPSNPC
license.txt	17,632	5668	7058	64	254
cs405(ei).txt	25,422	2654	88395	66	254
acread9.txt	35,121	447984	581067	73	255
deutsch.txt	47,829	685963	1840256	77	255
genesis.txt	49,600	3318506	6091523	75	255
pod.txt	69,981	694410	6916935	76	255
mspaint.txt	136,463	2667664	8608307	88	255
cmd.txt	152,028	2216429	9514025	73	245
d3dim.txt	193,189	906300	9930856	10	255
clbcataq.txt	403,901	3896171	9968012	11	255

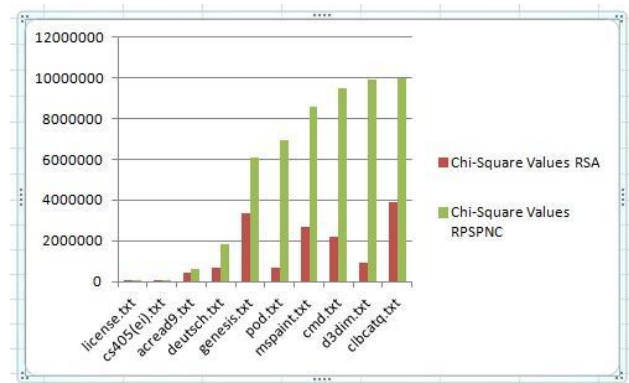


Fig 11. Graphical representation of Chi-Square value of RSA and RPSNPC

Table V shows the Chi-Square values of ten source files of RSA and RPSNPC. It is clearly observed that the extent of non-homogeneity of RPSNPC is quite higher than that of RSA. So, RPSNPC is giving optimal solution in terms of non-homogeneity by using Chi-Square values. Figure 11 shows the result graphically, from it is seen that that for all the ten source files the Chi-Square value of RPSNPC is quite higher than that of RSA. The degree of freedom of this RPSNPC is also quite higher than that of RSA.

D. TIME COMPLEXITY ANALYSIS

Another way to analyze any algorithm is to take the time complexity analysis [2,6]. Here encryption time and decryption time [2,6] have been taken into account.

Table VI
Encryption and decryption time of RSA and RPSNPC

Source File	File Size (Bytes)	Encryption Time		Decryption Time	
		RSA	RPSNPC	RSA	RPSNPC
license.txt	17,632	0.01	0.01	0.28	0.18
cs405(ei).txt	25,422	0.06	0.03	0.30	0.20
acread9.txt	35,121	0.07	0.05	1.67	0.90
deutsch.txt	47,829	0.11	0.10	3.51	2.90
genesis.txt	49,600	0.12	0.11	5.06	2.55
pod.txt	69,981	0.12	0.11	4.34	3.60
mspaint.txt	136,463	0.20	0.21	8.37	4.80
cmd.txt	152,028	0.25	0.21	6.59	6.33
d3dim.txt	193,189	0.28	0.23	10.15	8.68
clbcataq.txt	403,901	0.32	0.25	11.70	10.90

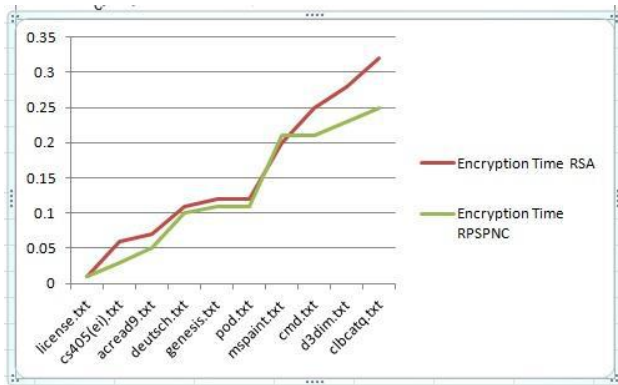


Fig 12. Graphical Representation of Encryption time



Fig 13. Graphical Representation of Decryption time

Table VI gives the tabulation for encryption time and decryption time of both RSA and RPSNPC. Figure 12 gives the graphical representation of encryption time and figure 13 gives the graphical representation of decryption time. The cumulative encryption time of RPSNPC is 1.49 seconds and the cumulative encryption time of RSA is 1.54 seconds. The cumulative decryption time of RPSNPC is 37.5 seconds and cumulative decryption time of RSA is 51.97 seconds. Therefore we can say that RPSNPC is giving much better result than that of RSA.

Table VII
The avalanche ratio of RSA and RPSNPC

Source File	File Size (Bytes)	Avalanche Ratio(in Percentage)	
		RSA	RPSNPC
license.txt	17,632	58.0	88.8
cs405(ei).doc	25,422	60.0	88.0
acread9.txt	35,121	75.0	88.8
deutsch.txt	47,829	78.9	95.5
genesis.txt	49,600	80.9	95.5
pod.exe	69,981	58.0	95.0
mspaint.exe	136,463	58.9	96.5
cmd.exe	152,028	67.0	95.0
d3dim.dll	193,189	67.9	95.0
clbcatq.dll	403,901	68.0	95.5

E. AVALANCHE RATIO TEST

The avalanche ratio test [6] is the extent of which the ciphertext bits flipped when one or more bits of plaintext or key are flipped.

Table VII is giving the avalanche ratio test and here RPSNPC is giving far better result than that of RSA.

VI. CONCLUSION

The technique given here is easily implemented in high level language and also in VHDL. This technique is very easy and it's implemented in FPGA-based systems, the goal of fast execution and strong cryptanalysis requirements are also obtained here. Moreover this technique can be fabricated in chip to be used in embedded systems. The main goal of the author is to develop an efficient FPGA-based crypto hardware and this is achieved through this proposed technique.

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Design of FPGA Based ECB Cryptosystem: RPPT Embedded with TB

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ABSTRACT

Cryptography is the method to implement security in computing systems. One of the methods is to design a cryptosystem, which is hardware/ Application-specific integrated circuit (ASIC) and performs fast encryption and decryption. Field-programmable gate array (FPGA) based cryptosystem is trending in recent research and development. This implementation is embedded approach and moreover electronic code block (ECB) approach is taken for final implementation. In TB, bits of the blocks are rearranged in a specific manner, for 4-bits, 8-bits, 16-bits, 32-bits and 64-bits block sizes. In RPPT, xor operation is performed from MSB to LSB of all the bits of particular blocks. In this paper, the main modification is in the implementation perspective. Novel three layer architecture is proposed where RPPT is embedded with TB, where n-bit block plaintext is first encrypted with TB, the resultant n-bit block is encrypted with RPPT and finally n-bit block is encrypted with TB. Many block cipher mode of operation is available, here ECB is chosen for the encryption and decryption. In TB, modification in orientation of bits has been done from original technique.
Keywords: FPGA-based-design, ECB, Embedded-technique, bit-level-implementation.

A. INTRODUCTION

Cryptosystem [3,4,5,6] is a special type of hardware or application specific IC which carries out fast encryption and decryption. Other advantages of cryptosystem are very low power consumption and low installation area as compared to software system. FPGA based cryptosystem [4,5] have become popular due to their very low production cost.

Cryptosystem can be implemented by two ways, first, symmetric key cryptosystem [1,2,3,6] and second, asymmetric key cryptosystem [1,2,3]. Symmetric key cryptosystem is much faster than that of asymmetric key cryptosystem. In this paper two symmetric key

techniques are used, RPPT [7] and TB [7]. Also RPPT is embedded [1] with TB; finally ECB [3] approach is taken to generate ciphertext [1,2,3,6]. This cryptosystem is successfully simulated in Spartan 3E FPGA [4] and software implementation have been also done for testing. This technique is compared with Rivest - Shamir - Adelman (RSA) algorithm [3] for its feasibility. Section II describes the technique, Section III deals with simulation, Section IV illustrates the results and Section V draws the conclusion.

II. THE TECHNIQUE

In this section the design process is illustrated. RPPT is described in section II.A, TB is described in section II.B, Embedded approach and ECB implementation is described in section II.C.

A. Recursive Pared Parity Technique (RPPT)

In RPPT, a new space efficient, universal encryption technique [1,2,3] have been suggested.

Consider a source sub-stream [1,2,3] (which is in binary representation) $B=(X_k, X_{k-1}, \dots, X_0)$, where X_{k-1} is the MSB and X_0 is the LSB.

Now, the transformation formula, which converts the source sub-stream to the immediate sub-stream are as follows:-

$$O_{k-1} = X_{k-1}$$

$$O_i = X_i \text{ xor } O_{i-1}, \text{ where } 1 \leq i \leq (K-2)$$

B. Transformation of Bits (TB)

The total message can be considered as a blocks of bits with different sizes like 2/4/8/16/32/64/128/256 [1,2,3]. The bit swapping can be applied to each block separately. The principle of bit swapping is discussed in following for different block sizes

Consider a block (X) with two binary bits [4,5] a and b:

$$X = ba$$

$$X1 = ab \quad \text{after 1}^{\text{st}} \text{ Swapping}$$

$$X2 = ba \quad \text{after 2}^{\text{nd}} \text{ Swapping}$$

It takes two swapping to get back the original block.

Consider a block (X) with four binary bits

$$X = dcba$$

$$X1 = cdab \quad \text{after 2 bit swapping on X}$$

$$X2 = abcd \quad \text{after 4 bit swapping on X1}$$

$$X3 = badc \quad \text{after 2 bit swapping on X2}$$

$$X4 = dcba \quad \text{after 4 bit swapping on X3}$$

It takes four swapping to get back the original block.

Consider a block (X) with eight binary bits

$$X = hgfedcba$$

$$X1 = ghfedcab \quad \text{after 2 bit swapping on X}$$

$$X2 = efghabcd \quad \text{after 4 bit swapping on X1}$$

$$X3 = abcdefgh \quad \text{after 8 bit swapping on X2}$$

$$X4 = badcfegh \quad \text{after 2 bit swapping on X 3}$$

$$X5 = dcbaghfe \quad \text{after 4 bit swapping on X 4}$$

$$X6 = ghfedcba \quad \text{after 8 bit swapping on X5}$$

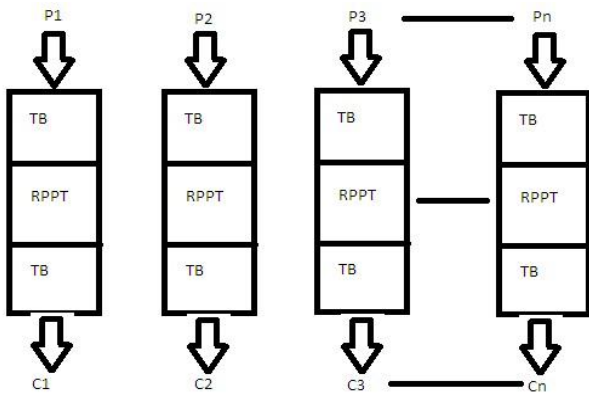


Fig. 1. Schematic diagram of final implementation

It takes six swapping to get back the original block.

In this way the above iterations are followed upto 128 bits. If the block size is 2^n then number of iterations [2] required to get back the original block [2] is $2 \times n$.

C. Implementation

This section describes the final implementation. Fig 1 shows the block diagram.

```

entity Encryption_Decryption is
  Port ( CLK : in STD_LOGIC;
        IN_DATA : in STD_LOGIC_VECTOR (63downto 0);
        OUT_DATA : out STD_LOGIC_VECTOR (63downto 0);
        EN_DN : in STD_LOGIC);
end Encryption_Decryption;
architecture Behavioral of Encryption_Decryption is
file IN_FILE:TEXT
  open READ_MODE is
  "D:\Xilinx14_VHDL_Projects\in.txt";
file OUT_FILE:TEXT
  open WRITE_MODE is
  "D:\Xilinx14_VHDL_Projects\out.txt";
signal BUFFER_STORE: std_logic_vector(63downto 0);
begin
process(CLK, EN_DN)
  variable BUF_IN, BUF_OUT: LINE;
  variable source_std_logic, destination_std_logic;
  buffer_std_logic: std_logic_vector(63downto 0);
begin
  if CLK'EVENT and CLK = '1' then
    if EN_DN = '1' or EN_DN = '0' then
      READLINE(IN_FILE, BUF_IN);
      READ(BUF_IN, source_std_logic);
      BUFFER_STORE <= TB_Three_Rounds(IN_DATA);
      buffer_std_logic :=
      TB_Three_Rounds(source_std_logic);
      BUFFER_STORE <= RPPT_Four_Rounds(BUFFER_STORE);
      buffer_std_logic :=
      RPPT_Four_Rounds(buffer_std_logic);
      OUT_DATA <= TB_Three_Rounds(BUFFER_STORE);
      destination_std_logic := TB_Three_Rounds(buffer_std_logic);
      WRITE(BUF_OUT, destination_std_logic);
      WRITELINE(OUT_FILE, BUF_OUT);
    end if;
  end if;
  file_close(IN_FILE);
  file_close(OUT_FILE);
end process;
end Behavioral;

```

Fig. 2. Top level VHDL module

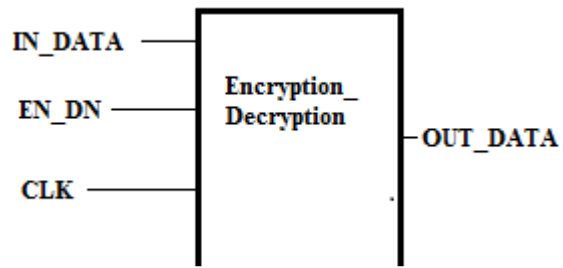


Fig. 3. Top level RTL module

The proposed technique is implemented by ECB mode. ECB is a mode of operation for a block cipher, with the characteristic that each possible block of plaintext has a defined corresponding cipher text value and vice versa. Electronic Code Book is used when a volume of plaintext is separated into several blocks of data, each of which is then encrypted independently of other blocks.

The message is considered as a plaintext [1,2,3] and is divided into n-numbers of blocks P1, P2, P3 Pn. Now, each encryption is consisting of three layer architecture. In the first layer TB is applied on Pk, then RPPT is applied on the resultant, finally TB is again applied on the resultant to generate cipher text block Ck.

This three layer architecture is embedded block cipher [1] and each Pk produces each Ck. Combining all C1, C2, C3 Cn finally ciphertext is generated. This process is also known as Electronic Code Block (ECB) [3] mode of operation.

III. SIMULATION

The proposed technique have been successfully simulated [4,5] for FPGA based system with IEEE VHDL (2002 standard) [5] and programmed in Xilinx ISE 14.2 [4,5].

Fig 2 shows the top level VHDL module [2,4,5]. Implementation is done with modular approach and same program is for RTL simulation [2,4,5] as well as file input and output.

Fig 3 shows the top level RTL module [2,4,5], where inputs are IN_DATA, EN_DN and CLK and OUT_DATA is output. During encryption IN_DATA is the plain text and OUT_DATA is the ciphertext. During decryption IN_DATA is ciphertext and OUT_DATA is plaintext. EN_DN value is 0 for encryption and 1 for decryption. CLK is the clock signal, encryption/decryption [1,2,3] is performed in positive/rising clock signal.

IV. RESULT

The proposed technique, for its feasibility, has been tested with RSA. Three parameters have taken for result and analysis.

TABLE I

	File name	File size	Entropy					
			Proposed Technique			RSA		
			Actual	Max	%	Actual	Max	%
1	Poppy.jpg	18kb	8.00	7.90	98.75	8.00	7.99	99.87
2	07.jpg	81KB	8.00	7.97	99.62	8.00	7.99	99.87
3	sqmapi.dll	131kb	8.00	6.60	82.5	8.00	7.98	99.75
4	Jview.exe	151kb	8.00	4.31	53.87	8.00	7.99	99.87
5	Gender.txt	207kb	4.70	2.54	54.04	8.00	7.99	99.87
6	Pod.exe	245kb	8.00	4.28	53.5	8.00	6.56	82
7	Devices.txt	303kb	4.70	2.92	62.12	8.00	7.99	99.87
8	DTLiteUI.dll	389kb	8.00	5.96	74.5	8.00	7.86	98.25
9	vssapi.dll	421kb	8.00	6.06	75.75	8.00	7.98	99.75
10	Names.txt	473kb	4.70	2.89	61.48	8.00	7.99	99.87

Entropy Test Analysis

Section IV.A discuss entropy test [3], section IV.B deals with the non-homogeneity test [2] and finally section IV.C illustrates the timing analysis [1,2,3].

A. Entropy Test

Truly random data has measurable characteristic called entropy. The term was coined in 1865 to describe a measure of the disorder of a thermodynamically system, and adapted by Shannon in 1948 as a measure of the unpredictability of information content.

Entropy is a function of the distribution. That is, the process used to generate a byte stream is what has entropy, not the byte stream itself. If it is given that the bits 1011, that could have anywhere from 0 to 4 bits of entropy; one have *no way* of knowing that value.

The entropy of a message is just the number of bits of information in the message, that is, the number of bits needed for the shortest possible encoding of the message. Here is the definition of Shannon entropy. Let X be a random variable that takes on the values.

$x_1, x_2, x_3, \dots, x_n$. Then the Shannon entropy is defined as

$$H(X) = -\sum \Pr[x_i] \cdot \log_2(\Pr[x_i])$$

Where $\Pr[x_i]$ represents probability.

With the aid of the information content of the individual messages, the average amount of information which a source with a specified distribution delivers can be calculated. To calculate this mean, the individual messages are weighted with the probabilities of their occurrence.

$$\text{Entropy}(\Pr[x_1], \Pr[x_2], \dots, \Pr[x_r]) := - [\Pr[x_1] * \log(\Pr[x_1]) + \Pr[x_2] * \log(\Pr[x_2]) + \dots + \Pr[x_r] * \log(\Pr[x_r])]$$

Note that the definition is a function of a random variable (i.e., a distribution), *not* a particular value. So, it can be said that lower is the entropy (inversely with probability of occurrence) higher is the randomness.

Table I shows the entropy test result. This test is done by Cryptool software. One input file is encrypted using RSA and then calculated entropy. In the next step the same input file is encrypted by proposed technique and then entropy is calculated from cipher text. It can be observed that entropy of the proposed technique is much lower than that of RSA. So, proposed technique is more random than that of RSA.

B. Non-Homogeneity Test

Non-homogeneity test is carried out using Pearson 's Chi-Square value. The Chi-squared Statistic is a measure of how similar two categorical probability distributions are. If the two distributions are identical, the chi-squared statistic is 0, if the distributions are very different, some higher number will result. The formula for the chi-squared statistic is:

$$X^2 = \sum_{i=1}^n \frac{(O_i - E_i)^2}{E_i}$$

O stands for the Observed frequency. E stands for the Expected frequency. Table II and fig 4 illustrates the result.

The observed frequency is the plaintext or ten source files. The expected frequency is the ciphertext or ten output files. Thus Chi-Square is calculated using above formulae.

Fig 4 is the logarithmic base 10 values of Chi-Square values of proposed technique and RSA. So, it can be seen that Chi-square values of proposed technique is quite higher than RSA for all ten files. It can be concluded proposed technique is more non-homogenous/heterogeneous than RSA. The degree of freedom of proposed technique is also higher than that of RSA.

C. Time Complexity Analysis

Time complexity analysis gives the efficiency of an algorithm means how much time an algorithm takes to generate correct output. Here posterior analysis of algorithm is used which directly depends on system and can measure only after running it on system. Therefore RSA and Proposed algorithm execution time notified on the same system to get the appropriate result. In time complexity analysis both encryption time and decryption time are taken. During analysis same file is taken as input for both the algorithm (RSA and Proposed) and calculate

the difference between end time and start time i.e. execution time of each algorithm. Table III illustrates the result.

TABLE II
Non-Homogeneity Test Analysis

Sr	File name	File size	Proposed Technique		RSA	
			Chi value	Degree of freedom	Chi value	Degree of freedom
1	Poppy.jpg	18kb	932	255	480	200
2	07.jpg	81K B	4196	255	2250	225
3	sqmapi.dll	131kb	453939	255	98760	220
4	Jview.exe	151kb	3577211	255	110750	215
5	Gender.txt	207kb	132754464	84	233805	88
6	Pod.exe	245kb	4223144	255	857800	215
7	Devices.txt	303kb	257540	65	923760	95
8	DTLiteUI.dll	389kb	3943211	255	1054675	225
9	vssapi.dll	421kb	1772858	255	1170567	235
10	Names.txt	473kb	61141140	89	3907850	90

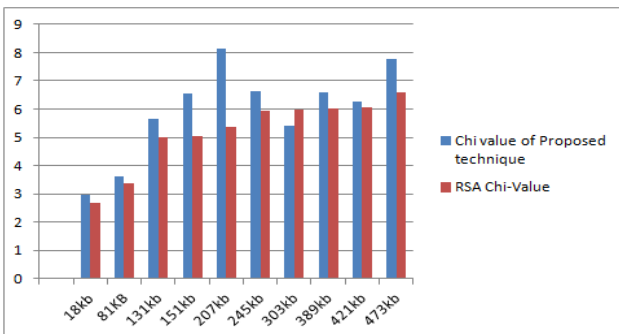


Fig. 4.Top level RTL module

TABLE III
Time Complexity Analysis

File Size (Bytes)	Encryption time (in Seconds)		Decryption time (in seconds)	
	RSA	Proposed Technique	RSA	Proposed Technique
17,632	0.01	0.01	0.28	0.01
25,422	0.03	0.02	0.30	0.02
35,121	0.21	0.02	1.67	0.02
47,829	0.35	0.03	3.51	1.00
49,600	0.40	0.02	5.06	0.95
69,981	0.39	1.00	4.34	0.98
136,463	0.65	1.01	8.37	1.00
152,028	0.61	1.01	6.59	1.01
193,189	0.75	0.99	10.15	1.02
403,901	0.95	1.00	11.70	1.05

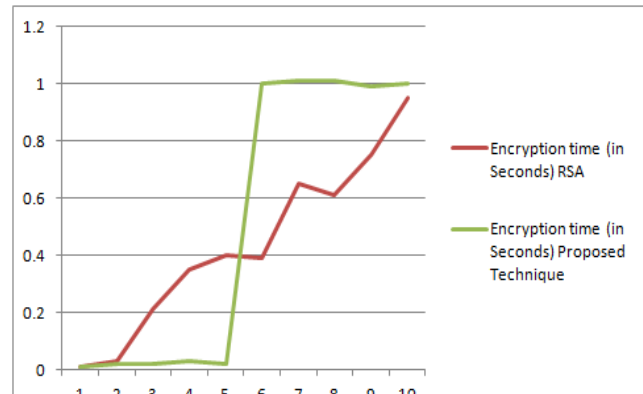


Fig. 5.Encryption time analysis

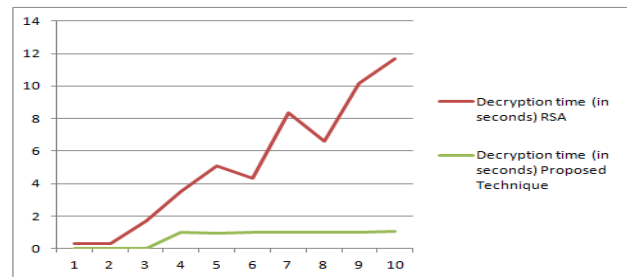


Fig. 6.Decryption time analysis

Fig 5 shows the encryption time analysis and Fig 6 shows the decryption time analysis. Observing both the figures time complexity of the proposed technique is quite less than RSA.

V. CONCLUSION

The proposed technique is successfully designed as a three layer embedded ECB cryptosystem. Proposed technique has been compared for entropy and non-homogeneity with RSA. These two are important cryptographic parameters. In algorithmic perspective the proposed technique has been compared for both encryption time and decryption time with RSA. All the testing results giving optimal result for this proposed technique. This proposed technique has also been successfully simulated for FPGA-based system. Thus with this proposed technique and or with little variation both software and hardware based security systems [3,4,5] can also be developed.

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