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PROFILE SUMMARY AND OBJECTIVE

Assistant Professor with 7+ years of experience in teaching and 10+ years of experience in research in the area of "Modeling and Simulation of nano dimensional devices and Low Power VLSI circuit designing" with 30+ publications in high impact factor journals and international conferences. Looking for opportunities to leverage my knowledge and experience as an Assistant Professor in Electronics and Communication Engineering.

PROFESSIONAL EXPERIENCE

- Presently working as an Assistant Professor in the Department of Electronics and Communication Engineering, Netaji Subhash Engineering College since July 2016.
- Worked as a Senior Research Fellow in the Department of Electronics and Telecommunication Engineering, Jadavpur University from December 2013- June 2016.

EDUCATIONAL BACKGROUND

- Ph.D. (Engg.) from Jadavpur University in 2019.
- M.Tech. in VLSI Design and Microelectronics Technology from Jadavpur University (Gold Medalist) in 2013.
- B.Tech. in Electronics and Communication Engineering from Maulana Abul Kalam Azad University of Technology (previously West Bengal University of Technology) in 2009.

AWARDS AND HONOURS

- *'Best Paper Award'* at 5th International Conference "2023 Devices for Integrated Circuit (DevIC)", at Kalyani Government Engineering College from 7-8 April, 2023 for the paper "Analytical Model of Dual Cavity Nanowire Tunnel FET-based Dielectric Modulated Biosensor".
- '*Best Paper Award'* at Springer International Conference on Communication Devices and Networking (ICCDN) 2017 organized by Sikkim Manipal Institute of Technology, Sikkim from 3rd to 4th June, 2017 for the paper "Analytical Modeling and Simulation of Triple Metal Front Gate Stack DG- MOSFET with Graded channel (GC-TMDG MOSFET)".
- Fellowship from Govt. of West Bengal under State Research Fellowship scheme.
- Gold Medal for securing the top position in M.Tech. in VLSI Design and Microelectronics Technology in the Department of ETCE, Jadavpur University.

- Prestigious memento from the Jawaharlal Nehru Memorial Fund, Govt. Of India, as recognition for excelling in the M.Tech. course at Jadavpur University.
- Fellowship from UGC UPE Phase II, Govt. of India.

MEMBERSHIP IN PROFESSIONAL BODIES

- Senior Member of the Electron Device Society of Institute of Electrical and Electronics Engineers (IEEE), USA (Membership #93324153).
- Advisor of IEEE Electron Devices Society Student Branch Chapter, NSEC since 2017.
- Treasurer, IEEE Electron Devices Society Kolkata Chapter (2020-2022)

REVIEWER

- Reviewer of Journal of Physics D: Applied Physics, IOP.
- Reviewer of Silicon, Springer.
- Reviewer of Journal of Computational Electronics, Springer.
- Reviewer of International Journal of High Speed Electronics and Systems (IJHSES).
- Reviewer of Computers and Electrical Engineering, Elsevier.

RESEARCH AREA

- Compact modeling and simulation of gate engineered nano dimensional field effect transistors.
- Low power VLSI circuit designing.

COURSES UNDERTAKEN

- Electronic Devices
- Analog Electronic circuits
- Digital Systems Design
- Digital Signal Processing
- CMOS VLSI Design
- Control System and Instrumentation
- Neural Network and Fuzzy Logic Control

DEPARTMENTAL ACTIVITIES

- Co-convenor of Departmental Academic Committee, ECE, NSEC
- Member of Student Affair Committee, ECE, NSEC.
- Member of Departmental R&D Committee, ECE, NSEC

ORGANIZING CAPABILITY as IEEE EDS SBC Advisor

1. IEEE EDS Distinguished Lecture (one day webinar) on "Redesigning Physical Electronics" on 18th December, 2021, by IEEE EDS Distinguished Lecturer, Prof. Muhammad Mustafa Hussain, UC Berkeley and EECS, KAUST, Saudi Arabia. The online platform chosen for this event was ZOOM Meetings.
2. A 2-day student – led workshop on 29 and 30 of October, 2021 on "Introduction to Electronics and VLSI (with introduction to HDL using Verilog)"
3. Conducted an introductory session on the "Benefits of IEEE EDS Student Branch Chapter" on April 20,2021.
4. Organized a one day webinar having two lecture series on "Tunnel FETs: Opportunities, Trends and Challenges" by Prof. Angsuman Sarkar, Department of Electronics & Communication Engineering, Kalyani Government Engineering College and on "Emerging Trends in Device Engineering for Improved Performances" by Dr. Navjeet Bagga, PDPM IIITDM Jabalpur, India on 4th March, 2021.
5. Organized an IEEE EDS one day webinar on "Ultra Low Power Logic Circuit Design Using Adiabatic Logic" on 13th February,2021by Dr. Manash Chanda, Assistant Professor, MSIT, Kolkata, and Vice Chairman, IEEE ED Kolkata Chapter.
6. Organized an IEEE EDS DL (one day webinar) on "Si-Based Resonant Interband Tunnel Diodes for Quantum Functional and Multi-Level Circuitry to Extend CMOS" on 13th February,2021,by IEEE EDS Distinguished Lecturer, Prof. Paul R. Berger, Director, Organic and Printed Flexible Electronics Laboratory, Department of Electrical and Computer Engineering, The Ohio State University.
7. Organized a one day webinar on "Signal Processing Tools for Condition Monitoring of Biomedical Systems" on 18th October,2020 by Mr. Saptarshi Chatterjee, Visvesvaraya PhD fellow, Electrical Engineering Department, Jadavpur University.
8. Organized a two-day webinar on "*4G and 5G Security-Opportunities and Challenges"* on 26th and 27th September,2020 by Dr. Ashutosh Dutta, senior scientist and 5G Chief Strategist at Johns Hopkins University, USA.
9. Organized a "One-day seminar on Machine Learning for IoT Analytics" by Prof. Amlan Chakrabarti, Professor and Director, A.K. Chowdhury School of Information Technology, University of Calcutta on 27th January 2020 at the Seminar Hall, Dept. of ECE, NSEC.
10. Organized an IEEE EDS Distinguished lecture on "GaN-HEMT based front end transceiver for 5G communication technology" by Dr. Ajit Kumar Panda, Professor and Dean, National Institute of Science and Technology, Berhampore on 17th January, 2020 at the Seminar Hall, Dept. of ECE, NSEC.
11. Organized a "One Day Hands-on Workshop in Embedded System and related use Cases" on 09.11.2019 in the Seminar Hall, Dept. of ECE, NSEC.
12. Organized an IEEE EDS Distinguished Lecture on "Circa 70 – Si Device Progression and Challenges towards Nanoera" on 2nd September 2019 by Dr. M.K. Radhakrishnan , Founder Director of NanoRel LLP, Singapore and is currently the Vice-President, IEEE Electron Devices Society (Regions and Chapters).

13. Organized a one day seminar on “Applied Data Science in Biology” on 4th April, 2019 by Dr. Parikshit Sanyal, Govt. of India.
14. Organized a one day seminar on “Recent trends in IT industry and how to motivate oneself to cope with it” on 1st March, 2019 by industry experts from Tata Consultancy Services emphasizing on Cloud computing, Bigdata, data mining, AI, Analytics, Automation.
15. Organized an IEEE EDS Distinguished Lecture on ' Next Generation Nanoelectronic Devices ' on 12th January 2019 by EDS Distinguished Lecturer Dr. Durga Misra Professor and Associate Chair for Graduate Studies, Electrical and Computer Engineering Department, New Jersey Institute of Technology (NJIT), USA sponsored by the IEEE Electron Devices Society under its Distinguished Lecturer Program.
16. Organized an IEEE EDS Distinguished Lecture on ' Recent advances in Tunnel Field Effect Transistor for sensing applications' on 24th November 2018 by EDS Distinguished Lecturer Dr. Manoj Saxena (Associate Professor, Department of Electronics, Deen Dayal Upadhyaya College, University of Delhi) sponsored by the IEEE Electron Devices Society under its Distinguished Lecturer Program.
17. Organized a one day seminar on ‘VLSI Circuits and applications in industry’ where Mr. Sayantan Sharangi, AMD India Pvt. Ltd. and Mr. Avishek Bhattacharya, Hewlett Packard Enterprise delivered their expert lectures on the mentioned topic on 10th October 2018 from 10 a.m. to 1 p.m. at APC Hall, NSEC.
18. Organized a workshop for students of A. K. Ghosh Memorial School, Lake Gardens, Kolkata on 14th September 2018 on “Familiarization with various electronic components and snap circuits” as an humanitarian activity of IEEE EDS-ETC (Engineers Demonstrating Science: an Engineer Teacher Connection) initiative to impart the knowledge of electronics among school students and introducing these budding talents into the world of electronics.
19. Organized a workshop for students of National Gems Higher Secondary School, Behala, Kolkata on 24thAugust 2018 on “Familiarization with various electronic components and snap circuits” as an humanitarian activity of IEEE EDS-ETC (Engineers Demonstrating Science: an Engineer Teacher Connection) initiative to impart the knowledge of electronics among school students and introducing these budding talents into the world of electronics.
20. Organized a one day seminar on ‘5G Communications’ on 4th August 2018 from 11 a.m. – 1 p.m. at the Language Lab II, NSEC where Dr. Ashutosh Dutta from Johns Hopkins University Applied Physics Labs (JHU/APL), New Jersey, USA delivered his valuable talk on “Security in SDF/NFV and 5G networks-Opportunities and Challenges” as an activity of IEEE EDS Student Branch Chapter, NSEC.
21. Organized a one day seminar on ‘Nanoscale Semiconductor Devices’ on 3rd May 2018 from 4 p.m. – 5 p.m. at the APC Hall, NSEC where Prof. Abhijit Biswas from Institute of Radiophysics and Electronics, University of Calcutta delivered his valuable talk on “MOSFETs and Emerging Hybrid CMOS Devices” as an activity of IEEE EDS Student Branch Chapter, NSEC.
22. Organized a one day seminar on ‘Electron Devices and Applications 2018’ on 20th March 2018 from 4 p.m. – 5 p.m. at the Seminar room, Department of Electronics and Communication Engineering, NSEC where Dr. Soumya Pandit from Institute of Radiophysics and Electronics, University of Calcutta delivered his valuable talk

on “Nano-scale MOS Transistor: Challenges and Solution Approaches” as an activity of IEEE EDS Student Branch Chapter, NSEC.

OTHER ORGANIZING CAPABILITY

1. Session chair and Technical Program Committee member at 5th International Conference “2023 Devices for Integrated Circuit (DevIC 2023)”, Kalyani Government Engineering College from April 7-8, 2023, organized by IEEE KGEC Student Branch Chapter in association with Department of ECE, KGEC and technically co-sponsored by IEEE EDS Kolkata Chapter.
2. Session chair and Technical Program Committee member at 4th International Conference “2021 Devices for Integrated Circuit (DevIC 2021)”, Kalyani Government Engineering College from May 19-20, 2021, organized by IEEE KGEC Student Branch Chapter in association with Department of ECE, KGEC and technically co-sponsored by IEEE EDS Kolkata Chapter.
3. Invited talks and tutorials co-chair at IEEE International Conference for Convergence in Engineering from 5th to 6th September 2020 organized by Netaji Subhash Engineering College, Kolkata.
4. Organizing Co-Chair at 2nd IEEE International Conference VLSI Devices Circuits and Systems (VLSI DCS 2020) from 21st to 22nd March 2020 organized by IEEE EDS Student Branch Chapter of Meghnad Saha Institute of Technology, Kolkata.
5. Organizing committee member at one-day seminar on ‘Circuits and Devices 2017’ on 22nd September, 2017 under the initiative of IEEE Student branch of Netaji Subhash Engineering College in association with IEEE EDS Kolkata Chapter.
6. Organizing committee member at one day workshop on ‘Remote Sensing and Applications 2017’ on 7th September 2017 organized by IEEE Student branch of Netaji Subhash Engineering College.

FACULTY DEVELOPMENT PROGRAMS/ SEMINARS/WORKSHOPS

1. Participated in the “3rd One Week Workshop on VLSI Device, Circuit and System Design Tools (Online)”, organized by the School of Electronics Engineering (SENSE), VIT-AP University, Amaravati (AP), India during 27th June to 3rd July, 2023.
2. Participated in the INUP - i2i Familiarization Workshop on Nanofabrication Technologies-- Ideas to Innovation, held at IIT Bombay during January 19-21, 2022.
3. Participated in International Symposium on History and Future of Transistors organized by IEEE Electron Device Society (EDS) Delhi Chapter, The National Academy of Sciences India (NASI)-Delhi Chapter and Deen Dayal Upadhyaya College during 23.12.2021-31.12.2021 using Digital Platform.
4. Attended the Faculty Development Program on 5G Communications and IoT held on 19th August, 2021 organized by Netaji Subhash Engineering College in association with TCS using Digital Platform.

5. Attended the five-day Faculty Development Program on “Machine Learning-Foundation, Methodologies and Interconnections” held during 16th – 21st August 2021 organized by Amity Institute of Information Technology, Amity University, Kolkata, using Digital Platform.

CERTIFICATIONS IN OTHER DOMAINS:

1. Completed a Coursera 4-week course on Programming for everybody (Getting Started with python)
2. Completed a Coursera course on Deep Learning

BOOKS/ BOOK CHAPTERS

1. Co-authored a chapter in the book titled "Low-Dimensional Nanoelectronic Devices: Theoretical Analysis and Cutting-Edge Research", CRC Press, Taylor and Francis, October 2022.
2. Co-authored a chapter in the book titled "Nanoelectronics -: Physics, Materials and Devices", Elsevier, January 2023.

PUBLICATIONS

Journals:

1. Rittik Ghosh, **Saheli Sarkhel** and Priyanka Saha, " Design and analysis of Z shaped $InGa_{0.5}As_{0.5}$/Si tunnel FET using non-equilibrium Green’s function model for hydrogen gas sensing application", **Micro and Nanostructures**, Elsevier, In press, July 2023 (**SCI, IF:3.22)**.
2. Koyel Mukherjee, Trisha Sau, Sneha Upadhyay, Susmita Mitra, Arpita Bhowmik, **Saheli Sarkhel**, Soumya Pandit, Rajat Kumar Pal, "A 588 nW, 1 nA current reference circuit with extremely low (0.002%/V) line sensitivity over a wide supply voltage range and low temperature coefficient", **Int. Journal of Numerical Model., Wiley**, Vol. 35, Issue 4, 2022. (**SCI, IF: 1.6)**.
3. Toushik Santra, Ankit Dixit, Rajeewa Kumar Jaisawal, Sunil Rathore, **Saheli Sarkhel** and Navjeet Bagga, "Investigation of geometrical impact on a P+ buried negative capacitance SOI FET", **Microelectronics Journal**, Elsevier, Volume 130, 2022. (**SCIE, IF: 2.2)**
4. Priyanka Saha , **Saheli Sarkhel** and Subir Kumar Sarkar "Two-Dimensional Potential and Threshold Voltage Modeling of Work Function Engineered Double Gate High-k Gate Stack Schottky Barrier MOSFET", **Journal of Electronic Materials**, Springer, Vol.8, Issue 6, pp-3823-3832, March 2019 (**SCI, IF:2.1)**.
5. **Saheli Sarkhel**, Priyanka Saha and Subir Kumar Sarkar, “Exploring the Threshold Voltage Characteristics and Short Channel Behavior of Gate Engineered Front Gate Stack MOSFET with Graded Channel”, **Silicon, Springer publications**, Volume 11, Issue 3, pp 1421–1428, June 2019. **(SCIE, IF- 3.4).**
6. Priyanka Saha, **Saheli Sarkhel** and Subir Kumar Sarkar ,“3D Modeling and Performance Analysis of Dual Material Tri Gate Tunnel Field Effect Transistor”, in **IETE Technical Review, Taylor and Francis,** Vol.36 Issue 2, pp-1-13,March 2018 **(SCIE, IF – 2.4).**
7. Priyanka Saha, **Saheli Sarkhel** and Subir Kumar Sarkar , "Compact 2D threshold voltage modeling and performance analysis of ternary metal alloy work-function-engineered double-gate MOSFET", in **Journal of Computational Electronics, Springer**, Vol.16.No.3,pp-648-657, June 2017 (**SCIE , IF: 2.1**).
8. Ranita Saha, **Saheli Sarkhel** and Subir Kumar Sarkar, "Analytical Modeling and performance characterization of a Double Gate MOSFET with Dielectric Pockets incorporating workfunction engineered binary metal alloy gate electrode for subdued SCEs", in **IETE Technical Review, Taylor and Francis**, Vol. 35, Issue 5, pp-506-513, 2017 (**SCIE, IF – 2.4**)
9. **Saheli Sarkhel,** Navjeet Bagga and Subir Kumar Sarkar, " A compact analytical model of binary metal alloy silicon-on-nothing (BMASON) tunnel FET with interface trapped charges" in **Journal of Computational Electronics**, Springer, September 2017, Volume

16, Issue 3, pp 704–713 (**SCIE , IF: 2.1**)

10. Navjeet Bagga, **Saheli Sarkhel** and Subir Kumar Sarkar. "Exploring the asymmetric characteristics of a Double Gate MOSFET with Linearly Graded Binary Metal Alloy Gate Electrode for enhanced performance." In **IETE Journal of Research, Taylor and Francis,** Volume 62, 2016 - Issue 6, Pages 786-794 , 2016 **(SCIE, IF – 1.5).**

11. **Saheli Sarkhel,** Navjeet Bagga and Subir Kumar Sarkar. "Compact 2D Modeling and Drain Current Performance Analysis of a Work Function Engineered Double Gate Tunnel Field Effect Transistor." In **Journal of Computational Electronics, Springer,** Vol. 15, Issue 1, pp. 104-114, March 2016 **(SCIE , IF: 2.1).**

12. **Saheli Sarkhel** and Subir Kumar Sarkar. "A compact quasi 3D threshold voltage modeling and performance analysis of a novel linearly graded binary metal alloy quadruple gate MOSFET for subdued short channel effects." In **Superlattices and Microstructures**, **Elsevier**, Vol. 82, pp. 293-302, 2015 **(SCI, IF – 3.22).**

13. **Saheli Sarkhel** and Subir Kumar Sarkar. "A comprehensive two dimensional analytical study of a Nanoscale Linearly Graded Binary Metal Alloy Gate Cylindrical Junctionless MOSFET for improved short channel performance." In **Journal of Computational Electronics, Springer**, Vol.13, pp. 925-932, 2014 **(SCIE , IF: 2.1).**

14. **Saheli Sarkhel**, Bibhas Manna and Subir Kumar Sarkar. "Threshold voltage modeling and performance comparison of a novel linearly graded binary metal alloy gate junctionless double gate metal oxide semiconductor field effect transistor." In **Indian Journal of Physics, Springer,** Vol. 89, No.6, pp. 593–598, 2015 **(SCIE, IF – 2.0).**

15. **Saheli Sarkhel**, Bibhas Manna and Subir Kumar Sarkar. "A Compact Two Dimensional Analytical Modeling of Nanoscale Fully Depleted Dual Material Gate strained SOI/SON MOSFETs for subdued SCEs." In **Journal of Low Power Electronics, ASP**, Volume 10, Number 3, pp. 383-391, September 2014. (**ESCI, Scopus Indexed, IF-0.84**)

16. **Saheli Sarkhel**, Bibhas Manna and Subir Kumar Sarkar. "Analytical Modeling and Simulation of a Linearly Graded Binary Metal Alloy Gate Nanoscale Cylindrical MOSFET for reduced short channel effects" In **Journal of Computational Electronics, Springer**, Vol. 13, No. 3, pp. 599-605, April, 2014. **(SCIE , IF: 2.1)**

17. **Saheli Sarkhel**, Bibhas Manna, P.K. Dutta and Subir Kumar Sarkar. "Analytical Model for performance comparison of a nano scale Dual Material Double Gate Silicon on Insulator (SOI) and Silicon on Nothing (SON) MOSFET." In **Journal of Nano Engineering and Nano Manufacturing, ASP,** Vol.4, No. 3, pp. 182-188, 2014.

18. Bibhas Manna, **Saheli Sarkhel**, Ankush Ghosh, S. S. Singh and Subir Kumar Sarkar. "Dual Material Gate Nanoscale SON MOSFET: For Better Performance." In **International Journal of Computer Application (IJCA)**, ISBN: 973-93-80875-27-15, 2013.

19. Bibhas Manna, **Saheli Sarkhel**, N. Islam, S. Sarkar and Subir Kumar Sarkar. "Spatial Composition Grading of Binary Metal Alloy Gate Electrode for Short-Channel SOI/SON MOSFET Application." In **IEEE Transaction on Electron Devices**, Vol-59, Issue-12, pp. 3280-3287, 2012. **(SCI, IF – 3.1)**

20. **Saheli Sarkhel,** Sounak Naha and Subir Kumar Sarkar "Reduced SCEs in Fully Depleted Dual-Material Double-Gate (DMDG) SON MOSFET: Analytical Modeling and Simulation." In **International Journal of Scientific and Engineering Research,** Volume 3, Issue 6, June 2012 Edition.

Conferences:

1. Ilika Mitra, Wasim Habib, Silpi Sarkar, **Saheli Sarkhel** and Soumya Pandit, "An approach for modeling propagation delay of a subthreshold inverter incorporating DIBL effect", 5th International Conference "2023 Devices for Integrated Circuit (DevIC)", at Kalyani Government Engineering College from 7-8 April, 2023, organized by IEEE KGEC Student Branch Chapter in association with Department of ECE, KGEC and with technical partnership from IETE Kolkata Chapter and IEEE EDS Kolkata Chapter.
2. **Saheli Sarkhel**, Sunil Rathore, Priyanka Saha, Ankit Dixit, Taha Saquib, Rajeewa K. Jaiswal, P.N. Kondekar and Navjeet Bagga, "Analytical Model of Dual Cavity Nanowire Tunnel FET-based Dielectric Modulated Biosensor", 5th International Conference "2023 Devices for Integrated Circuit (DevIC)", at Kalyani Government Engineering College from 7-8 April, 2023, organized by IEEE KGEC Student Branch Chapter in association with Department of ECE, KGEC and with technical partnership from IETE Kolkata Chapter and

IEEE EDS Kolkata Chapter.

3. Sneha Upadhyay, Trisha Sau, Susmita Mitra, Arpita Bhowmik, Saheli Sarkhel and Soumya Pandit, "Statistical Analysis of a Low Power Analog Current Source", 3rd IEEE Conference on VLSI Device, Circuit and System (VLSI DCS 2022) to be organized by Meghnad Saha Institute of Technology, Kolkata during 19th -20th January, 2022.
4. Saheli Sarkhel, Riya Rani Dey, Soumyarshi Das, Sweta Sarkar, Toushik Santra and Navjeet Bagga, "A Novel Dual Metal Double Gate Grooved Trench MOS Transistor: Proposal and Investigation", 2nd International Conference on Frontiers in Computing and Systems (COMSYS-2021) during 29th September to 1st October 2021 organized by Department of Electronics & Communication Engineering and Department of Information Technology North-Eastern Hill University (A Central University), Shillong, Meghalaya, India.
5. Taha Saquib, **Saheli Sarkhel** and Soumya Pandit, "A 0.6 V 1.6 nA Constant Current Reference with Improved Power Supply Sensitivity", 4th International Conference "2021 Devices for Integrated Circuit (DevIC 2021)", Kalyani Government Engineering College from May 19-20, 2021, organized by IEEE KGEC Student Branch Chapter in association with Department of ECE, KGEC and technically co-sponsored by IEEE EDS Kolkata Chapter.
6. **Saheli Sarkhel** and Navjeet Bagga, "Analytical Model of a Strain Induced Lateral Channel Workfunction Engineered Surrounding Gate MOSFET", IEEE Conference on Applied Signal Processing, ASPCON 2020, 7th – 9th October, 2020, Jadavpur University.
7. Rishov Aditya, **Saheli Sarkhel** and Soumya Pandit, "Comparative Study of Doublet OTA Circuit Topologies Operating in Weak Inversion Mode for Low Power Analog IC Applications", IEEE EDS conference VLSI DCS 2020 on July, 2020 at Meghnad Saha Institute of Technology, Kolkata.
8. Priyanka Saha, Saheli Sarkhel, Pritha Banerjee, Subir Kumar Sarkar, "3D Modeling based Performance Analysis of Gate Engineered Trigate SON TFET with SiO_2/HfO_2stacked gate oxide", 2018 IEEE International Conference on Electronics, Computing and Communication Technologies (CONECCT), Bangalore, 16-17 March 2018.
9. **Saheli Sarkhel**, Priyanka Saha, Pritha Banerjee and Subir Kumar Sarkar, " Two dimensional analytical modeling based threshold voltage characteristics of proposed linearly graded work function engineered gate all around SB MOSFET", IEEE International Conference on Computing, Power And Communication Technologies 2018 (GUCON) organized by Galgotias University, Noida on September 28-29, 2018.
10. Priyanka Saha, **Saheli Sarkhel**, Dinesh Kumar Dash, Suvam Senapati and Subir Kumar Sarkar, "Analytical Modeling and Simulation of Triple Metal Front Gate Stack DG- MOSFET with Graded channel (GC-TMDG MOSFET)", Springer International Conference on Communication Devices and Networking (ICCDN) 2017, Sikkim Manipal Institute of Technology, Sikkim from 3rd to 4th June, 2017. (**Best Paper Awarded**)
11. **Saheli Sarkhel**, Priyanka Saha and Subir Kumar Sarkar, "Parasitic Fringe Capacitance Modeling of Work Function Engineered Double Gate TFET", in the 2nd IEEE International Conference "**Devices for Integrated Circuits (DevIC 2017)**", Kalyani Government Engineering College from March 23-24, 2017.
12. Navjeet Bagga, **Saheli Sarkhel** and Subir Kumar Sarkar. "Analytical Model for ID-VD characteristics of a Triple Metal Double Gate TFET." In **IEEE International Conference on Computing, Communication and Automation (ICCCA 2016)**, 29th-30th April 2016, Noida.
13. **Saheli Sarkhel**, Navjeet Bagga and Subir Kumar Sarkar. "Analytical Modeling and Simulation of Work-function Engineered Gate Junctionless high-k dielectric Double Gate MOSFET: A Comparative Study." In **Michael Faraday IET International Summit-2015 (MFIIS 2015)**, An IET International Conference 12th -13th September, 2015, Kolkata.
14. Navjeet Bagga, **Saheli Sarkhel** and Subir Kumar Sarkar. "Recent Research Trends in Gate Engineered Tunnel FET for Improved Current Behaviour by subduing the Ambipolar Effects: A Review." In **IEEE International Conference on Computing, Communication and Automation (ICCCA2015)** 15th -16th May 2015, Noida.
15. **Saheli Sarkhel**, Bibhas Manna and Subir Kumar Sarkar. "A Compact Capacitive Approach based Threshold Voltage Modeling and Performance Comparison of a novel UBR MOSFET with SOI MOSFET." In **2nd International Conference on Devices, Circuits and Systems (ICDCS 2014), IEEE Conference**, 6-8 March, 2014, Coimbatore.
16. Kousik Naskar, Anindya Jana, **Saheli Sarkhel**, Bibhas Manna and Subir Kumar Sarkar. "Study of power dissipation and delay of two dimensional SOI-SON based MOSFET inverter." In **2013 Annual International Conference on Emerging Research Areas and 2013**

International Conference on Microelectronics, Communications and Renewable Energy (AICERA/ICMiCR), IEEE Conference, June 4-6, 2013, Kerala.

17. Anindya Jana, Kousik Naskar, **Saheli Sarkhel**, Bibhas Manna, J.K. Singh and Subir Kumar Sarkar. "Realization of Gate performance of OR gate using hybrid Pass transistor based logic circuit." In **2013 Annual International Conference on Emerging Research Areas and 2013 International Conference on Microelectronics, Communications and Renewable Energy (AICERA/ICMiCR), IEEE Conference**, June 4-6, 2013.Kerala.

18. **Saheli Sarkhel**, Bibhas Manna, Anindya Jana, Kousik Naskar and Subir Kumar Sarkar. "Analytical Potential Distribution Model of Symmetric Double Gate Underlap MOSFET with Binary Metal Alloy as Gate Electrode for Subdued SCEs." In **2013 Annual International Conference on Emerging Research Areas and 2013 International Conference on Microelectronics, Communications and Renewable Energy (AICERA/ICMiCR), IEEE Conference**, June 2013, Kerala.

19. Deepon Saha, Kousik Naskar, **Saheli Sarkhel**, Bibhas Manna and Subir Kumar Sarkar. "Device Circuit Co-Design of FD-SON MOSFET using BSIMSOI MOSFET Model." In **2013 IEEE International Conference on Electronics, Computing and Communication Technologies (CONECCT 2013), IEEE Conference**, 17-19 January,2013, IISc Bangalore.

20. Tiya Dey Malakar, Bibhas Manna, **Saheli Sarkhel**, Sourav Naskar, P. K. Dutta and Subir Kumar Sarkar. "Small - Signal Parameter Extraction to Study the RF Performance of SOI and SON MOSFET." In **2012 International Conference on Communications, Devices and Intelligent Systems (CODIS 2012), IEEE Conference,** 28-29 December 2012, Jadavpur University, Kolkata.

21. Sounak Naha, **Saheli Sarkhel** and Subir Kumar Sarkar. "A Two Dimensional Analytical Modeling of Fully Depleted Dual Material Gate SON MOSFET and Evidence for Suppressed SCEs." In **1st International Conference on Devices, Circuits and Systems (ICDCS 2012), IEEE Conference**, March 15-16, 2012, Karunya University, Coimbatore.